



## GENERAL DESCRIPTION

The RZC6601Q is a fast charging protocol controller for HiSilicon Fast Charging Protocol (FCP) and QC 2.0/3.0 USB interface. The RZC6601Q monitors USB D+/D- data line and automatically adjusts the output voltage depending on different powered device (PD). The charging time of PD is therefore optimized by the RZC6601Q.

RZC6601Q can support not only USB BC compliant devices, but also Apple / Samsung / HUAWEI devices and automatically detects whether a connected powered device is QC 2.0/3.0 or FCP capable before enabling output voltage adjustment. If a PD is not compliant with QC 2.0/3.0 and FCP, the RZC6601Q will disable the adjustment of output voltage and keep the default 5V output voltage for safe operation.

The RZC6601Q is available in a space-saving SOT23-6 package.

## FEATURES

- Supports HiSilicon Fast Charging Protocol (FCP)
- Supports Qualcomm® Quick Charge™ 2.0/3.0  
Class A : 3.6V up to 12V Output Voltage
- Automatically Selects FCP and QC2.0/3.0 Protocols
- Supports USB DCP Shorting D+ Line to D- Line per USB Battery Charging Specification, Revision 1.2
- Complies with Chinese Telecommunication Industry Standard YD/T 1591-2009
- Supports USB DCP Applying 2.7V on D+ Line and 2.7V on D- Line

## APPLICATIONS

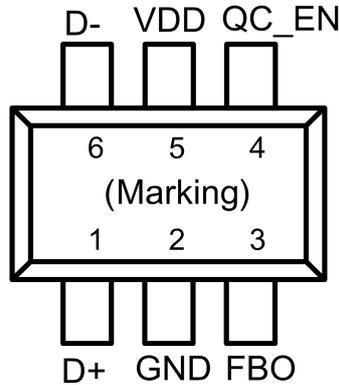
- Wall-Adapter, Smart Phones, Tablets, Notebooks
- Mobile / Tablet Power Bank
- Car Charger
- USB Power Output Ports

## ORDERING INFORMATION

Part Number	Package	Top Marking	Packing
RZC6601Q	SOT23-6	6601Q1F Or FRC1F	3000PCS/Real



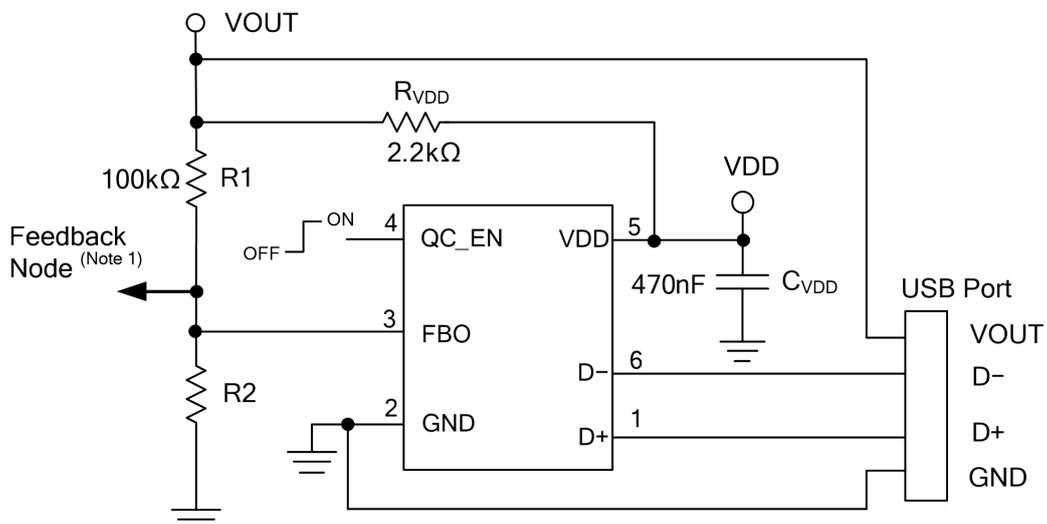
## PIN ASSIGNMENTS



## FUNCTIONAL PIN DESCRIPTION

Pin Name	Pin No.	Pin Function
D+	1	USB D+ data line. Recommended this pin connect without resistors(open) or with a resistor higher than 1MΩ connect to GND.
GND	2	Ground pin.
FBO	3	Feedback output pin. Current sink/source FB node.
QC_EN	4	QC_enable: QC2.0/3.0 and FCP function are enabled by either logic high or high-Z. Contrarily, QC2.0/3.0 and FCP function are disabled by logic low.
VDD	5	Power supply input pin.
D-	6	USB D- data line.

## TYPICAL APPLICATION CIRCUIT



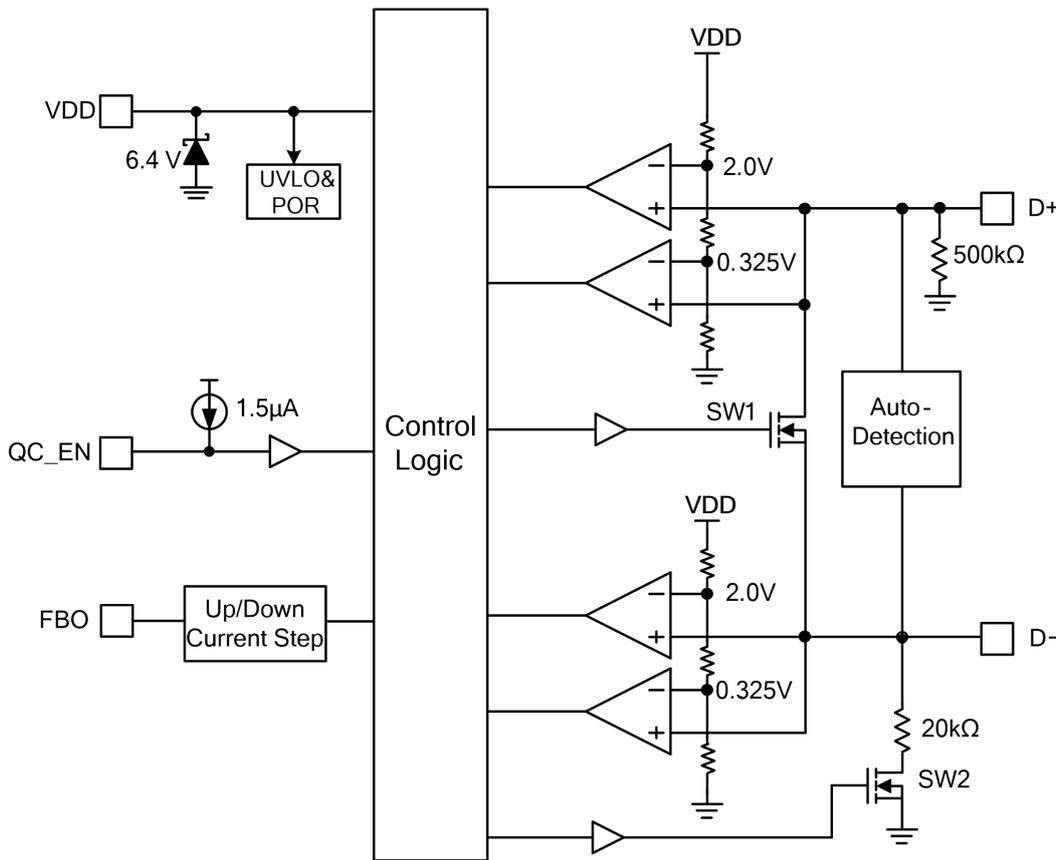
Note 1: The recommended voltage of feedback node ranges between 0.4V and 1.5V



**OUTPUT VOLTAGE LOOKUP TABLE (QC 2.0/3.0)**

D+	D-	Output Voltage
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Continuous mode
0.6V	High-Z	5V (Default)

**BLOCK DIAGRAM**





## ABSOLUTE MAXIMUM RATINGS (Note 2)

- Input Supply Voltage VDD ----- -0.3V to +7V
- D+,D-Pins Voltage ----- -0.3V to +14V
- All Other Pins Voltage ----- -0.3V to +7V
- Maximum Junction Temperature ( $T_J$ )----- +150°C
- Storage Temperature ( $T_S$ )----- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ----- +260°C
- Package Thermal Resistance, ( $\theta_{JA}$ ) (Note 3)
  - SOT-23-6----- 250°C/W
- Package Thermal Resistance, ( $\theta_{JC}$ )
  - SOT-23-6----- 110°C/W

Note 2: Stresses beyond this listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Note 3:  $\theta_{JA}$  is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

## RECOMMENDED OPERATING CONDITIONS

- Input Supply Voltage (VDD)----- +3.2V to +6.8V
- Operation Temperature Range ( $T_{OPR}$ ) ----- -40°C to +85°C



## ELECTRICAL CHARACTERISTICS

(VDD=5V, TA=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Input Section</b>						
VDD Input Voltage Range	V <sub>DD</sub>		3.2		6.8	V
Input UVLO Threshold	V <sub>UVLO(VTH)</sub>	V <sub>DD</sub> Falling	2.5		2.9	V
VDD Supply Current		V <sub>DD</sub> =5V, Measure V <sub>DD</sub>		180		μA
VDD Shunt Voltage	V <sub>DD(SHUNT)</sub>	I <sub>VDD</sub> = 3mA	5.9	6.4	6.8	V
<b>High Voltage Dedicated Charging Port (HVDCP)</b>						
Data Detect Voltage	V <sub>DAT(REF)</sub>		0.25	0.32 5	0.4	V
Output Voltage Selection	V <sub>SEL_REF</sub>		1.8	2.0	2.2	V
D+ High Glitch Filter Time	T <sub>GLITCH(BC)-D+_H</sub>		1000	125 0	150 0	ms
D- Low Glitch Filter Time	T <sub>GLITCH(BC)-D-_L</sub>			1		ms
Output Voltage Glitch Filter Time	T <sub>GLITCH(V)CHANGE</sub>		20	40	60	ms
D- Pull-Down Resistance	R <sub>D-(DWN)</sub>			20		kΩ
Continuous Mode Glitch Filter Time (Note 4)	T <sub>GLITCH-CONT-CHANGE</sub>		100		200	μs
D+ Leakage Resistance	R <sub>DAT-LKG</sub>	V <sub>DD</sub> =3.2-6.4V, V <sub>D+</sub> =0.6-3.6V	300	500	800	kΩ
Switch SW1 On-Resistance	R <sub>DS_ON_N1</sub>	V <sub>DD</sub> =5V, SW1= 200μA			40	Ω
Up/Down Current Step	I <sub>UP</sub> , I <sub>DOWN</sub>	I <sub>UP</sub> = 40μA (9V), 70μA (12V),		2		μA
Feedback Output Voltage	V <sub>FBO</sub>		0.4		1.5	V
<b>DCP Charging Mode</b>						
D+ <sub>-0.48V</sub> /D- <sub>-0.48V</sub> Line Output Voltage			0.44	0.48	0.52	V
D+ <sub>-0.48V</sub> /D- <sub>-0.48V</sub> Line Output Impedance				900		kΩ

**Electrical Characteristics (Continued)**(VDD=5V, T<sub>A</sub>=25°C and the recommended supply voltage range, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Apple Mode</b>						
D+ <sub>2.7V</sub> /D- <sub>2.7V</sub> Line Output Voltage			2.57	2.7	2.84	V
D+ <sub>2.7V</sub> /D- <sub>2.7V</sub> Line Output Impedance				33.6		kΩ
<b>D- SECTION (FCP)</b>						
D- FCP Tx Valid Output High	V <sub>TX-VOH</sub>		2.55		3.6	V
D- FCP Tx Valid Output Low	V <sub>TX-VOL</sub>				0.3	V
D- FCP Rx Valid Output High	V <sub>RX-VIH</sub>		1.4		3.6	V
D- FCP Rx Valid Output Low	V <sub>RX-VIL</sub>				1.0	V
D- Output Pull-Low Resistance (FCP) (Note 4)	R <sub>PD</sub>		400	500	600	Ω
Unit Interval For FCP PHY Communication	UI	f <sub>CLK</sub> = 125kHz	144	160	180	μs
<b>Others</b>						
QC_EN High-Level Input Voltage	V <sub>IH</sub>		1.2			V
QC_EN Low-Level Input Voltage	V <sub>IL</sub>				0.4	V



## APPLICATION INFORMATION

### FUNCTION DESCRIPTION

The RZC6601Q integrates both USB high voltage dedicated charging port interface IC for QC 2.0 and QC3.0 class A and HiSilicon FCP specification.

The RZC6601Q can fast charge most of the handheld devices. It could be treated as the original charging adapter.

The RZC6601Q supports BC1.2, Samsung and HUAWEI devices. It also supports output voltage range of QC 3.0 Class A (3.6V to 12V) or QC 2.0 Class A (5V, 9V, 12V).

### QUICK CHARGE 2.0/3.0 INTERFACE

When the RZC6601Q is powered on, D+ and D- pin are applied to 2.7V for Apple device. If handheld device has the function of QC 2.0/3.0, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will short to D- pin through the switch SW1 for entering BC 1.2. If D+ is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the RZC6601Q will enter QC 2.0/3.0 or FCP operation mode.

When the voltage of D+ pin and D- pin simultaneously satisfy these two inequalities  $V_{DAT(REF)} < D+ < V_{SEL\_REF}$  and  $D- > V_{SEL\_REF}$ , the RZC6601Q would enter continuous mode.

In the continuous mode, each voltage pulse on D+ pin generated by powered device is between 1V and 3V. In the meanwhile, the high level of pulse should be keep at least 200us. If the specified conditions are satisfied, the FBO pin will sink 2uA per pulse. The maximum sink current is 70uA for output voltage 12V.

In the continuous mode, each voltage pulse on D- pin generated by powered device is between 3V and 1V. At the same time, the low level of pulse should be keep at least 200us. If the specified conditions are satisfied, the FBO pin will source 2uA per pulse. The maximum source current is 14uA for output voltage 3.6V.

If the powered device doesn't support QC 2.0, the RZC6601Q will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than  $V_{DAT(REF)}$  and the output default voltage 5V is also applied.

### SHUNT REGULATOR

The VDD of RZC6601Q is supplied by the wide output voltage through the external resistor  $R_{VDD}$ . The internal Zener-Diode is utilized to clamp the VDD at 6.4V. The recommended value of  $R_{VDD}$  and  $C_{VDD}$  are 2.2k $\Omega$  and 470nF, respectively.

### QC\_EN FUNCTION

QC 2.0/3.0 and FCP function are disabled by connecting the QC\_EN pin to ground. On the contrary, QC 2.0/3.0 and FCP function could be enabled by connecting QC\_EN pin to VDD or high. Additionally, when RZC6601Q is already accessed QC 2.0/3.0 or FCP mode, the selected mode can't be changed by setting QC\_EN pin.



深圳市瑞之辰科技有限公司

RZC6601Q

*USB Charging Port Controller for Fast Charging Protocol*

## **DATA LINE PROTECTION**

When D+/D- pin is touched by the output voltage in abnormal situation, the D+/D- pin of both sink device and source device may be damaged. In order to protect the D+/D- pin of the devices from damage in abnormal situation, the RZC6601Q will return the output voltage to default output voltage 5V when the voltage of D+/D- pin is touched larger than 7.5V.



# PACKAGE INFORMATION

## SOT23-6

