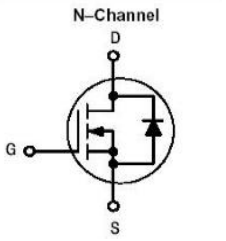
GENERAL DESCRIPTION

The RZC8012D is the high cell density trenched N-Channel MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The RZC8012D meet the ROHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

PIN CONFIGURATION



FEATURES

- 80V/75A, $R_{DS(ON)}$ =12mΩ V_{GS} = 10V (MAX.)
- 80V/75A, $R_{DS(ON)}$ =15mΩ V_{GS} = 4.5V (MAX.)
- 100% EAS Guaranteed
- Green Device Available
- Supper Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- TO-252 package design

APPLICTIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

ORDERING INFORMATION

Part Number	Package	Top Marking
RZC8012D	TO-252	D8012

MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol		Value	Units
Drain to Source Voltage	V_{DSS}		80	V
Gate to Source Voltage	V_{GSS}		±20	V
Continuous Drain Current	25℃	I_D	75	A
	70℃		60	A
Pulsed Drain Current	$I_{D(pulse)}$		200	A
Maximum Power Dissipation	25℃	P_D	52	W
Single Pulse Avalanche Energy	EAS		80	mJ
Operating Junction Temperature	T_J		150	°C
Storage Temperature	T_{STG}		-55-+150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)	T_L		260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS (TA = 25℃)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{DS}=250uA	80			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=64V,V_{GS}=0V T_J=25°C			1	uA
		V_{DS}=64V,V_{GS}=0V T_J=55°C			5	uA
Gate Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	1.2		2.5	V
Drain to Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=20A		10	12	mΩ
		V_{GS}= 4.5V,I_D=10A		12	15	mΩ
Gate Resistance	Rg	V_{DS}=0V ,V_{GS}=0V , f=1MHz		0.66		Ω
Input Capacitance	C_{ISS}	V_{DS}=50V , V_{GS}=0V , f=1MHz		3120		pF
Output Capacitance	C_{OSS}			140		pF
Reverse Transfer Capacitance	C_{RSS}			110		pF
Total Gate Charge (10V)	Q_G	V_{DD}=64V , V_{GS}=4.5V , I_D=10A		61		nC
Gate-Source Charge	Q_{GS}			8.5		nC
Gate-Drain Charge	Q_{GD}			18		nC
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=40V, V_{GS}=10V RG=3.3Ω,I_D=10A		12		nS
Rise Time	Tr			25		
Turn-Off Delay Time	$T_{d(off)}$			51		
Fall Time	Tf			18		

Note : 1. Pulse test: pulse width <= 300us, duty cycle<= 2%.

2. Static parameters are based on package level with recommended wire-bonding.

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

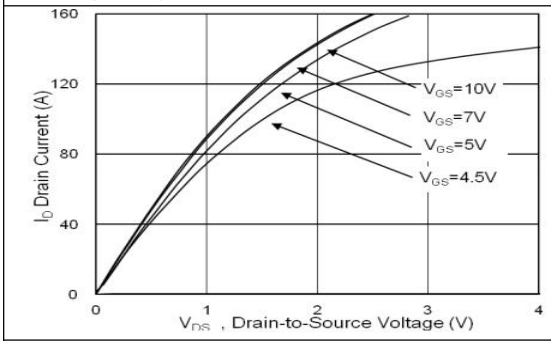


Fig 2. On-Resistance VS. V_{GS}

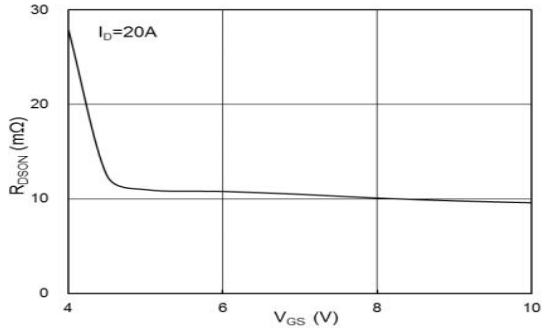


Fig 3. Forward Characteristics of Reverse

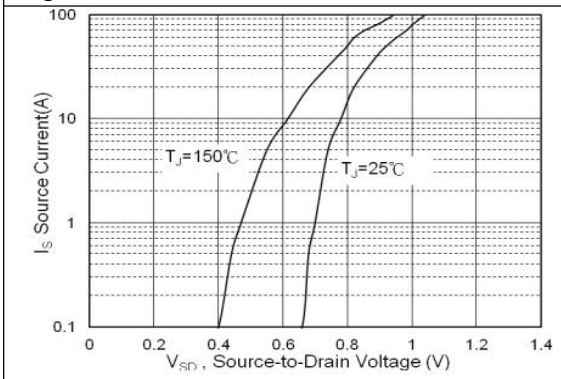


Fig 4. Gate-Charge Characteristics

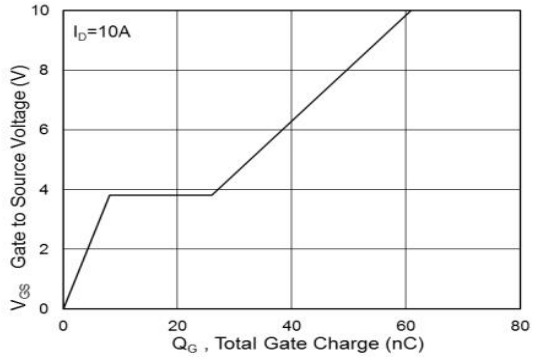


Fig.5 Normalized $V_{GS(TH)}$ VS. T_J

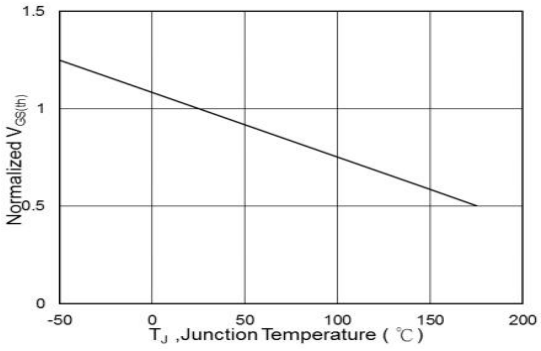


Fig.6 Normalized $R_{DS(ON)}$ VS. T_J

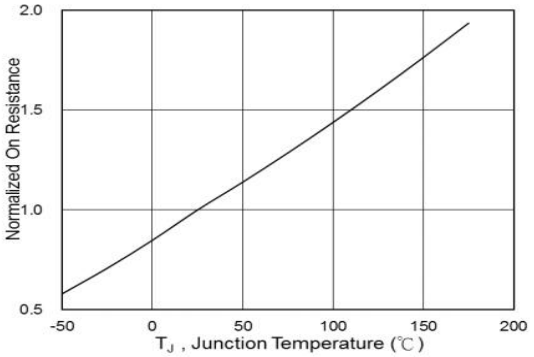


Fig.7 Capacitance

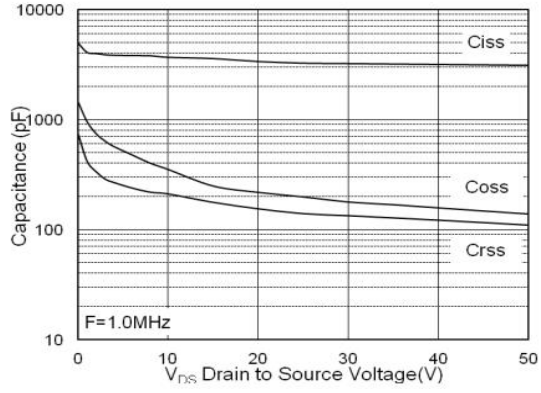


Fig.8 Safe Operation Area

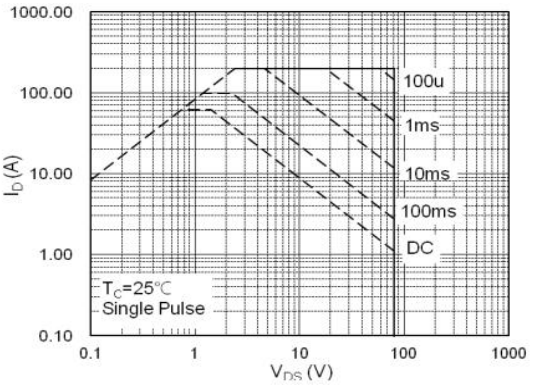
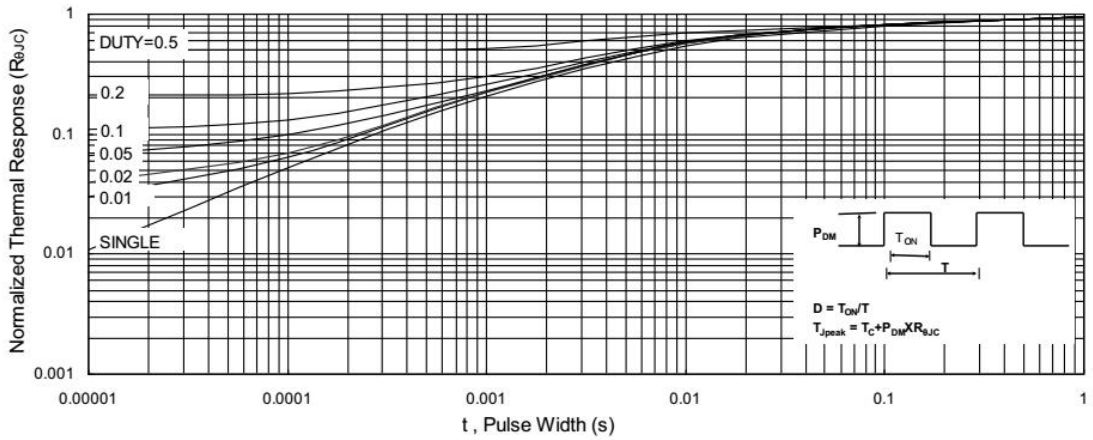
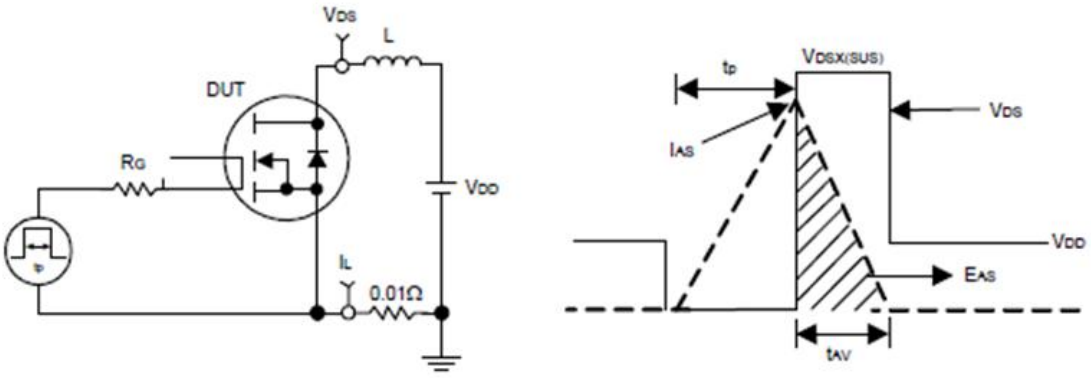


Fig.9 Normalized Maximum Transient Thermal Impedance

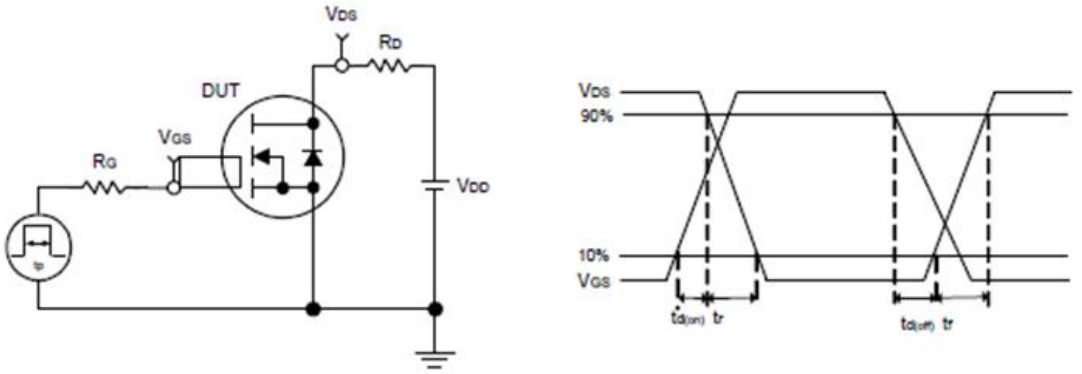


TEST CIRCUITS

Avalanche Test Circuit and Waveforms

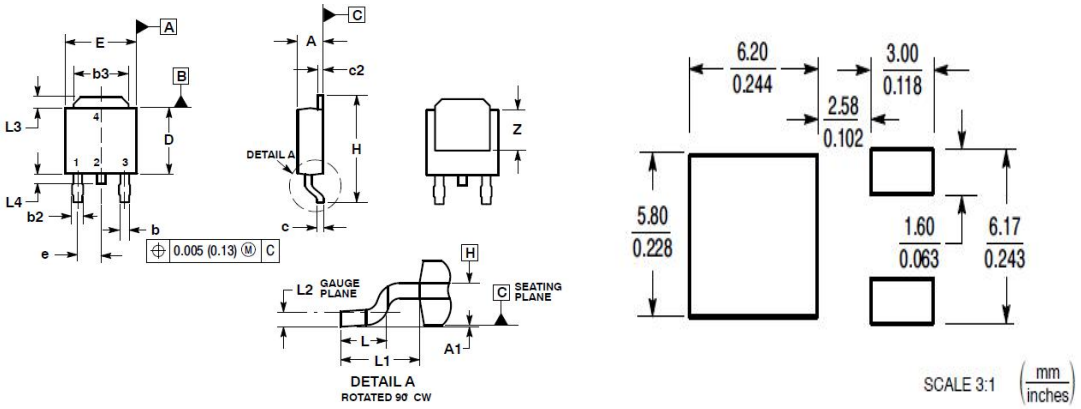


Switching Time Test Circuit and Waveforms



PACKAGE DIMENSIONS

TO-252



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---