

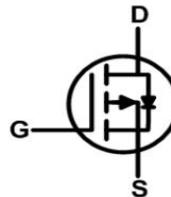


## GENERAL DESCRIPTION

The RZC6103D is the high cell density trench P-Channel MOSFET, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The RZC6103D meet the RoHS and Green Product requirement with full function reliability approved.

## PIN CONFIGURATION



## FEATURES

- -60V/-18A,  $R_{DS(ON)} = 65m\Omega$   $V_{GS} = 10V$  (TYP.)
- -60V/-18A,  $R_{DS(ON)} = 95m\Omega$   $V_{GS} = 4.5V$  (TYP.)
- 100% EAS Guaranteed
- Green Device Available
- Supper Low Gate Charge
- Excellent  $C_{dv/dt}$  effect decline
- Advanced high cell density Trench technology
- TO-252 package design

## APPLICTIONS

- Load Switch
- Battery Powered System
- Hard Switch and High Frequency Circuits
- UPS.

## ORDERING INFORMATION

Part Number	Package	Top Marking	Packing
RZC6103D	TO-252	D6103	2500PCS/Tape&Real

**MAXIMUM RATINGS** (Ta = 25°C)

Parameter	Symbol	Value	Units	
Drain to Source Voltage	V <sub>DSS</sub>	-60	V	
Gate to Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current	25°C	I <sub>D</sub>	-18	A
	70°C		-11	A
Pulsed Drain Current (note 1)	I <sub>D(pulse)</sub>	-36	A	
Single Pulse Avalanche Energy	E <sub>AS</sub>	35	mJ	
Avalanche Current	I <sub>AS</sub>	-26	A	
Maximum Power Dissipation	25°C   P <sub>D</sub>	34.7	W	
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	62	°C/W	
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	3.6	°C/W	
Operating Junction Temperature	T <sub>J</sub>	150	°C	
Storage Temperature	T <sub>STG</sub>	-55-+150	°C	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T <sub>L</sub>	260	°C	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

**ELECTRICAL CHARACTERISTICS** (TA = 25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX	Units
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>DS</sub> =-250uA	-60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V T <sub>J</sub> =25°C			-1	uA
		V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-5	uA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate threshold voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-2	-2.5	V
Drain to Source On-state Resistance <sup>(note 2)</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-12A		65	70	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-8A		95	105	mΩ
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		1447		pF
Output Capacitance	C <sub>OSS</sub>			97		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			70		pF
Total Gate Charge (-4.5V)	Q <sub>G</sub>	V <sub>DD</sub> =-48V , V <sub>GS</sub> =-10V , I <sub>D</sub> =-10A		9.86		nC
Gate-Source Charge	Q <sub>GS</sub>			3.08		nC
Gate-Drain Charge	Q <sub>GD</sub>			2.95		nC
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-1A		28.8		nS
Rise Time	T <sub>r</sub>			19.8		
Turn-Off Delay Time	T <sub>d(off)</sub>			60.8		
Fall Time	T <sub>f</sub>			7.2		
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C		-0.9	-1.2	V
Maximum Continuous Drain-Source Diode Forward Current	I <sub>D</sub>	T <sub>C</sub> =25°C			-18	A
Maximum Pulse Drain-Source Diode Forward Current	I <sub>DSM</sub>				-36	A

Note : 1.The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≤300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-25V, V<sub>GS</sub>=-10V, L=0.1mH, I<sub>AS</sub>=-26.6A

4.The power dissipation is limited by 150°C junction temperature

5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.



### TYPICAL CHARACTERISTICS

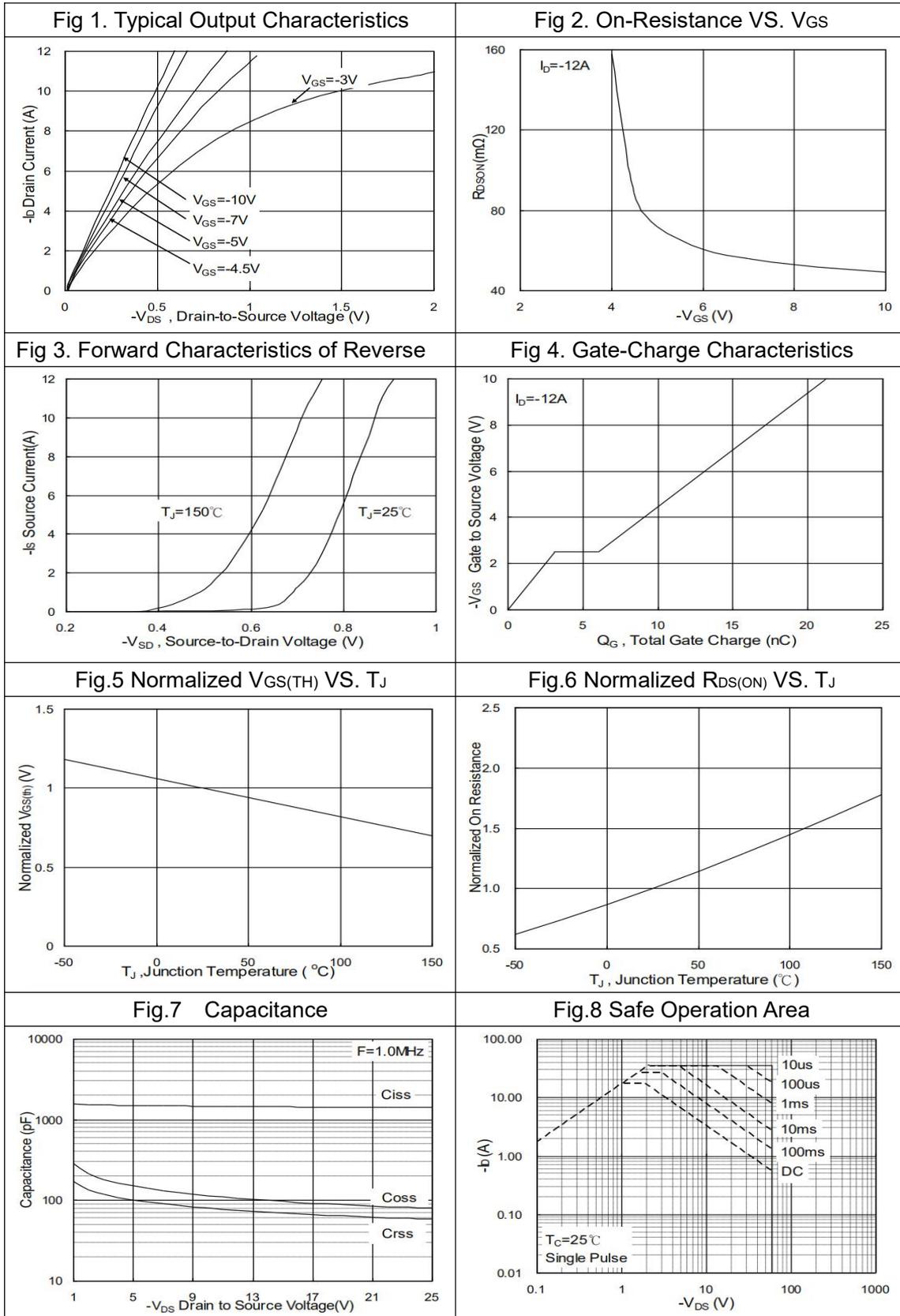
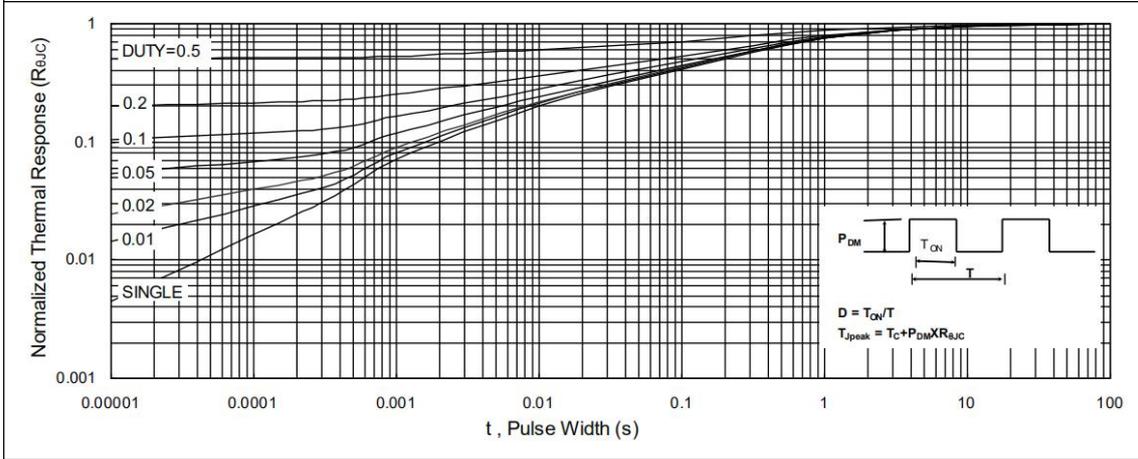




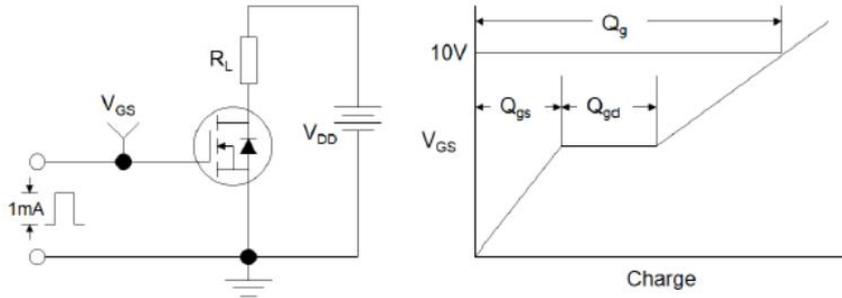
Fig.9 Maximum Effective Transient Thermal Impedance, Junction to Case



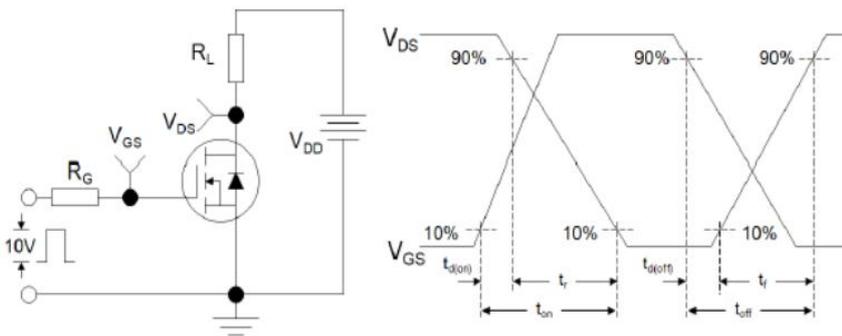


## TEST CIRCUITS

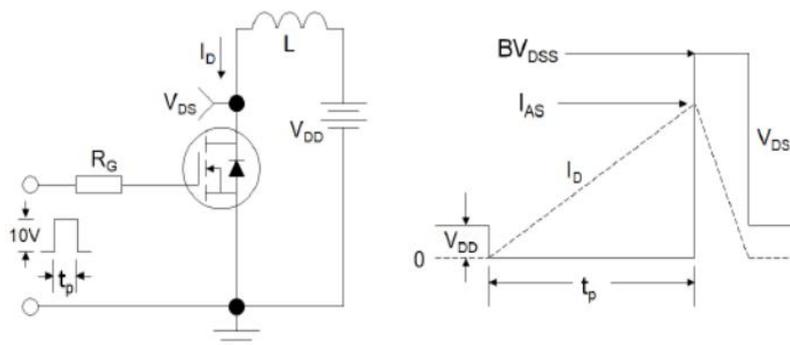
### Gate Charge Test Circuit and Waveform



### Resistive Switching Test Circuit and Waveform



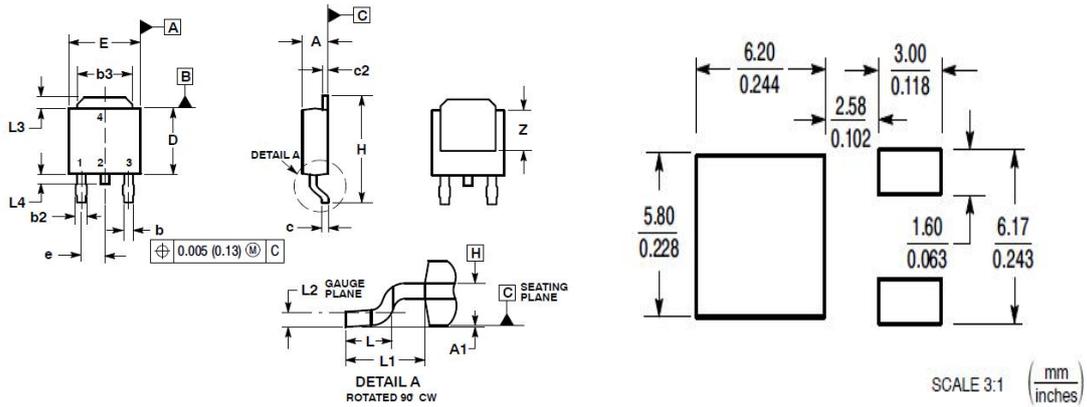
### Unclamped Inductive Switching Test Circuit and Waveform





PACKAGE DIMENSIONS

TO-252



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---