



## GENERAL DESCRIPTION

The RZC6007D is the high cell density trench N-Channel MOSFET, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The RZC6007D meet the ROHS and Green Product requirement with full function reliability approved.

## PIN CONFIGURATION



## FEATURES

- 60V/75A,  $R_{DS(ON)} = 7m\Omega$   $V_{GS} = 10V$  (TYP.)
- 60V/75A,  $R_{DS(ON)} = 9m\Omega$   $V_{GS} = 4.5V$  (TYP.)
- 100% EAS Guaranteed
- Green Device Available
- Supper Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- TO-252 package design

## APPLICTIONS

- Load Switch
- Battery Powered System
- Hard Switch and High Frequency Circuits
- UPS.

## ORDERING INFORMATION

Part Number	Package	Top Marking	Packing
RZC6007D	TO-252	D6007	2500PCS/Tape&Real

**MAXIMUM RATINGS** ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Value	Units
Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	25 $^\circ\text{C}$	75 A
		70 $^\circ\text{C}$	47 A
Pulsed Drain Current (note 1)	$I_{D(pulse)}$	280	A
Single Pulse Avalanche Energy	$E_{AS}$	80	mJ
Avalanche Current	$I_{AS}$	40	A
Maximum Power Dissipation	25 $^\circ\text{C}$   $P_D$	41	W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	62	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	1.4	$^\circ\text{C}/\text{W}$
Operating Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55-+150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

**ELECTRICAL CHARACTERISTICS** (TA = 25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX	Units
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>DS</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V T <sub>J</sub> =25°C			1	μA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			5	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate threshold voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	2	2.5	V
Drain to Source On-state Resistance <sub>(note 2)</sub>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		7	8.5	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A		9	12	mΩ
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =30V , V <sub>GS</sub> =0V , f=1MHz		3307		pF
Output Capacitance	C <sub>OSS</sub>			201		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			151		pF
Total Gate Charge (10V)	Q <sub>G</sub>	V <sub>DD</sub> =30V , V <sub>GS</sub> =10V , I <sub>D</sub> =18A		57		nC
Gate-Source Charge	Q <sub>GS</sub>			9		nC
Gate-Drain Charge	Q <sub>GD</sub>			14		nC
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω, I <sub>D</sub> =20A		16		nS
Rise Time	T <sub>r</sub>			41		
Turn-Off Delay Time	T <sub>d(off)</sub>			56		
Fall Time	T <sub>f</sub>			16		
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C		0.9	1.2	V
Maximum Continuous Drain-Source Diode Forward Current	I <sub>D</sub>	T <sub>C</sub> =25°C			75	A
Maximum Pulse Drain-Source Diode Forward Current	I <sub>DSM</sub>				280	A
Reverse Recovery Time	trr	I <sub>F</sub> =20A, T <sub>J</sub> =25°C Di/Dt=100A/μS		22		nS
Reverse Recovery Charge	Q <sub>rr</sub>			72		nC

Note : 1.The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≤300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=40A

4.The power dissipation is limited by 150°C junction temperature

5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.



### TYPICAL CHARACTERISTICS

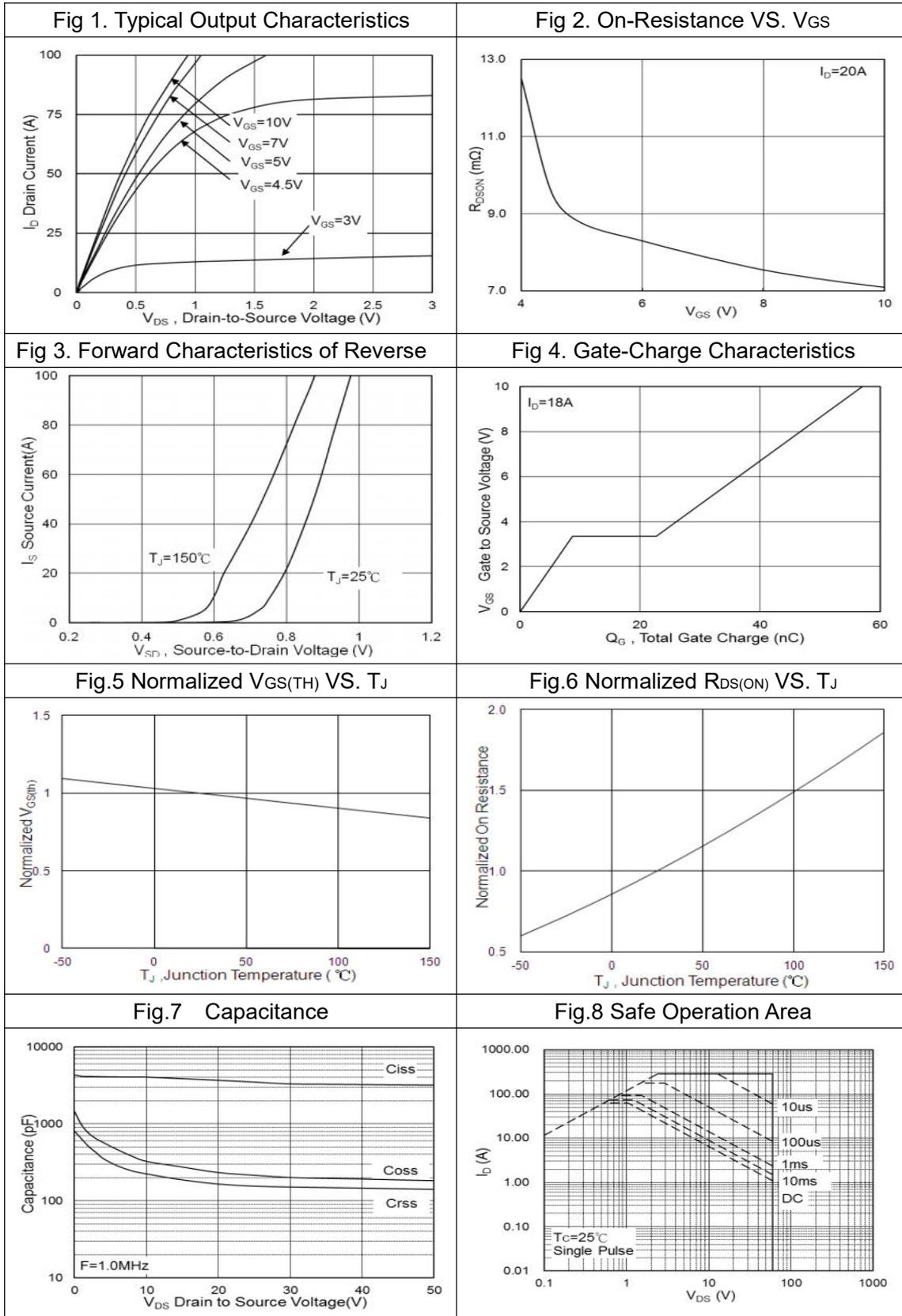
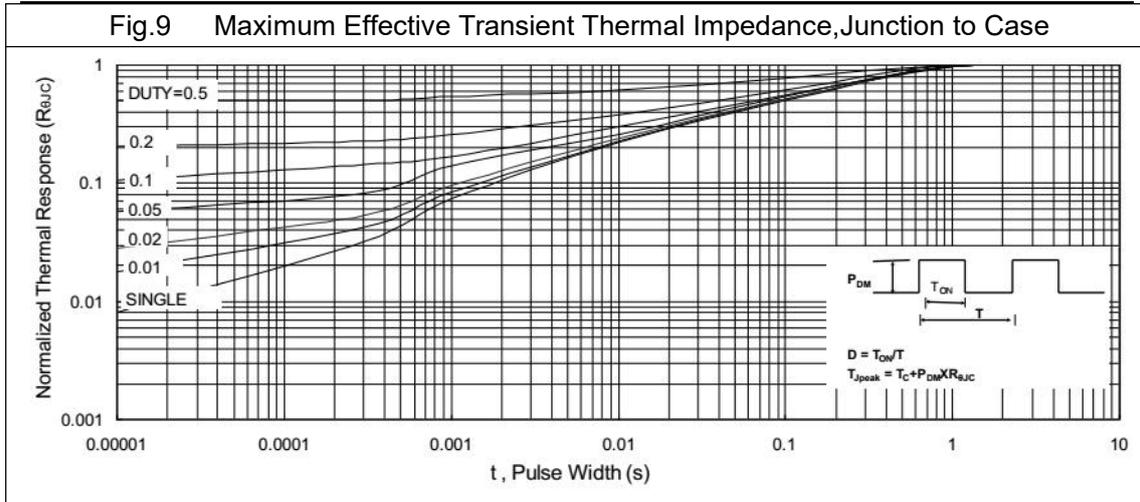




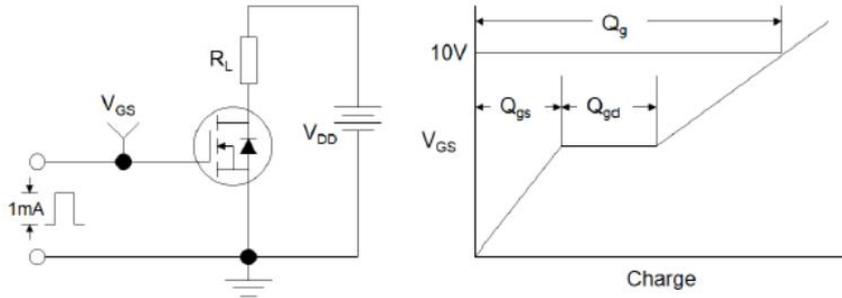
Fig.9 Maximum Effective Transient Thermal Impedance, Junction to Case



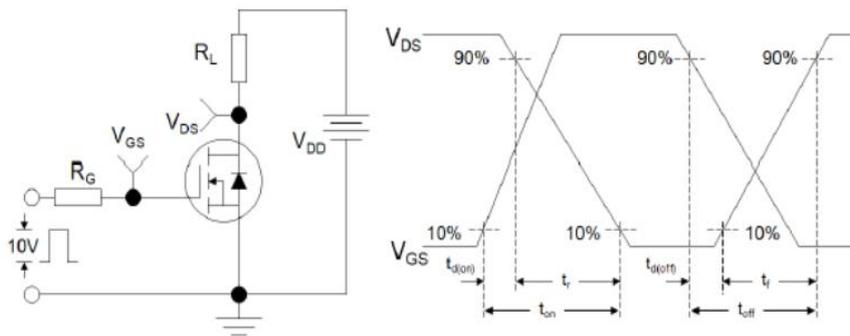


## TEST CIRCUITS

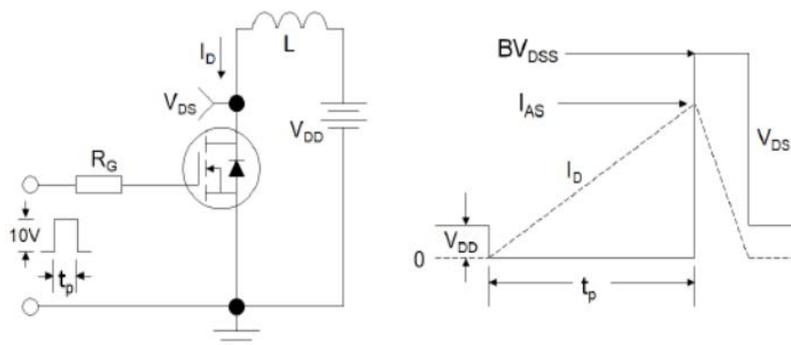
### Gate Charge Test Circuit and Waveform



### Resistive Switching Test Circuit and Waveform



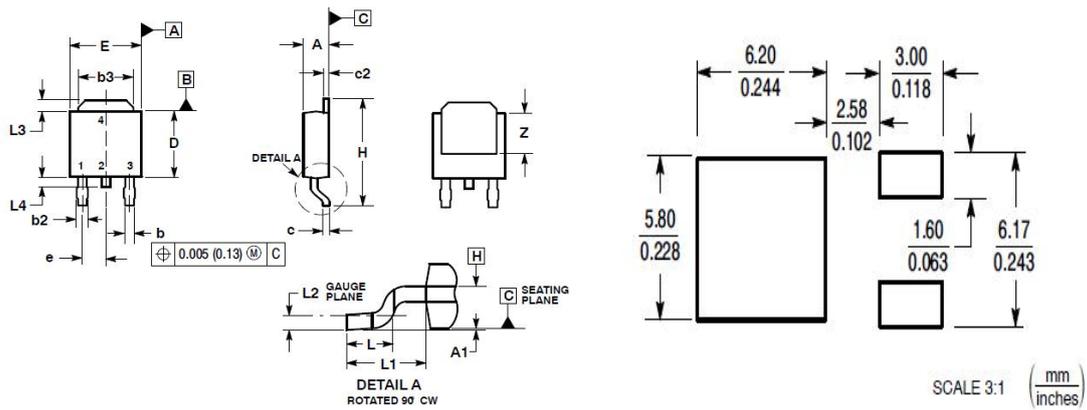
### Unclamped Inductive Switching Test Circuit and Waveform





PACKAGE DIMENSIONS

TO-252



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---