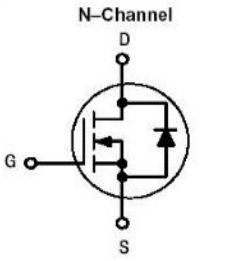
GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

PIN CONFIGURATION



FEATURES

- 60V/75A, $R_{DS(ON)}$ =5mΩ V_{GS} = 10V (TYP.)
- 60V/75A, $R_{DS(ON)}$ =6mΩ V_{GS} = 4.5V (TYP.)
- 100% EAS Guaranteed
- Green Device Available
- Supper Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- TO-252 package design

APPLICTIONS

- Load Switch
- Battery Powered System
- Hard Switch and High Frequency Circuits
- UPS.

ORDERING INFORMATION

Part Number	Package	Top Marking	Packing
RZC6005D	TO-252	D6005	2500PCS/Real

MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol		Value	Units
Drain to Source Voltage	V_{DSS}		60	V
Gate to Source Voltage	V_{GSS}		±20	V
Continuous Drain Current	25℃	I_D	75	A
	70℃		47	A
Pulsed Drain Current (note 1)	$I_{D(pulse)}$		300	A
Single Pulse Avalanche Energy	E_{AS}		181	mJ
Avalanche Current	I_{AS}		60	A
Maximum Power Dissipation	25℃	P_D	101	W
Thermal Resistance,Junction to Case	$R_{\theta JC}$		1.23	℃/W
Thermal Resistance,Junction to Ambient	$R_{\theta JA}$		62	℃/W
Operating Junction Temperature	T_J		150	°C
Storage Temperature	T_{STG}		-55-+150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)	T_L		260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS (TA = 25℃)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{DS}=250uA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V T_J=25°C			1	uA
		V_{DS}=48V,V_{GS}=0V T_J=125°C			10	uA
Gate Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.6	2.5	V
Drain to Source On-state Resistance(note 2)	$R_{DS(ON)}$	V_{GS}=10V,I_D=20A		5	6	mΩ
		V_{GS}= 4.5V,I_D=15A		6	7.5	mΩ
Input Capacitance	C_{ISS}	V_{DS}=25V , V_{GS}=0V , f=1MHz		4740		pF
Output Capacitance	C_{OSS}			325		
Reverse Transfer Capacitance	C_{RSS}			161		
Total Gate Charge (10V)	Q_G	V_{DD}=30V , V_{GS}=4.5V , I_D=10A		33		nC
Gate-Source Charge	Q_{GS}			11		
Gate-Drain Charge	Q_{GD}			12		
Turn-On Delay Time	$T_{d(on)}$	V_{DD}=15V,I_D=1A V_{GS}=10V,R_G=3.3Ω		20		nS
Rise Time	Tr			14.2		
Turn-Off Delay Time	$T_{d(off)}$			61		
Fall Time	Tf			16.8		
Drain-Source Diode Forward Voltage	V_{SD}	Is=1A,V_{GS}=0V, T_C=25℃			1.0	V
Maximum Continuous Drain-Source Diode Forward Current	I_D	T_C=25℃			75	A
Maximum Pulse Drain-Source Diode Forward Current	I_{DSM}				300	A

Note : 1.The data tested by surface mounted on a 1 inch$_2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≦300us , duty cycle ≦ 2%

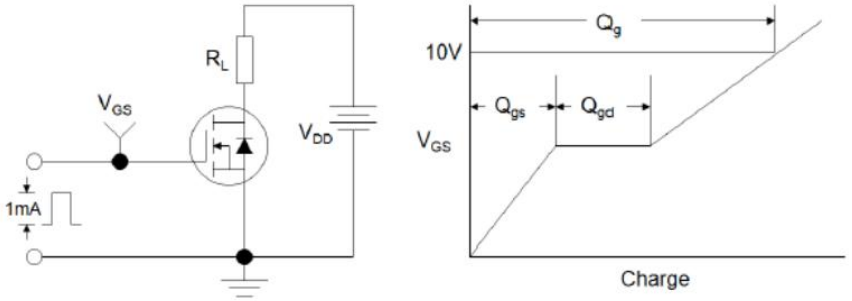
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=60A

4.The power dissipation is limited by 150℃ junction temperature

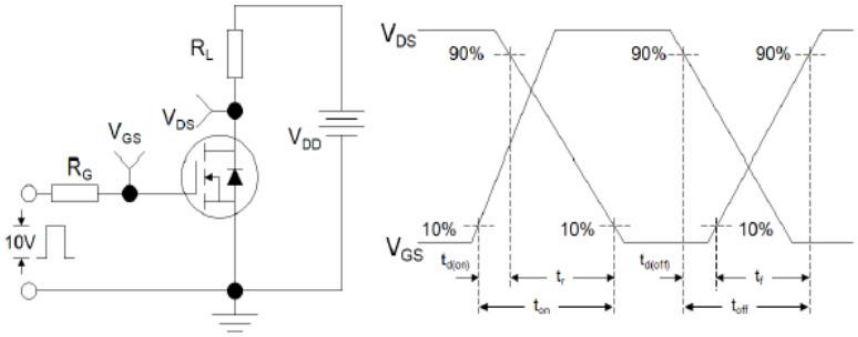
5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

TEST CIRCUITS

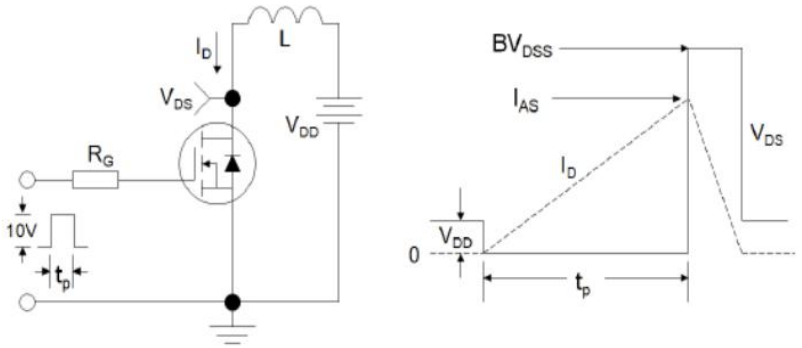
Gate Charge Test Circuit and Waveform



Resistive Switching Test Circuit and Waveform

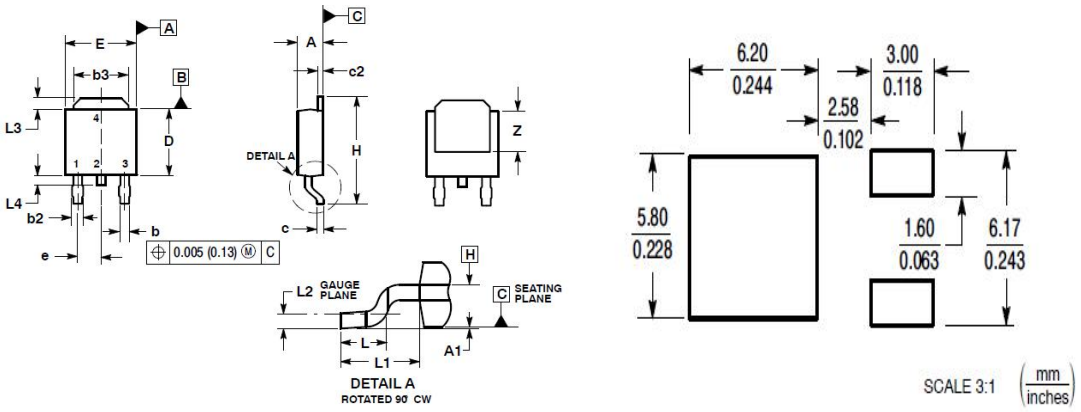


Unclamped Inductive Switching Test Circuit and Waveform



PACKAGE DIMENSIONS

TO-252



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---