

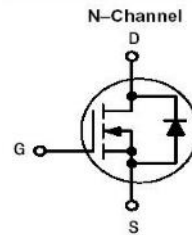
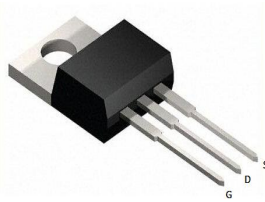


## GENERAL DESCRIPTION

The RZC4005T is the high cell density trenched N-Channel MOSFET, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The RZC4005T meet the ROHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

## PIN CONFIGURATION



## FEATURES

- 40V/90A,  $R_{DS(ON)} = 5\text{m}\Omega$   $V_{GS} = 10\text{V}$  (TPY.)
- 40V/90A,  $R_{DS(ON)} = 7\text{m}\Omega$   $V_{GS} = 4.5\text{V}$  (TPY.)
- 100% EAS Guaranteed
- Green Device Available
- Supper Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology
- TO-220 package design

## APPLICTIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

## ORDERING INFORMATION

Part Number	Package	Top Marking
RZC4005T	TO-220	T4005

**MAXIMUM RATINGS** ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Value	Units	
Drain to Source Voltage	$V_{DSS}$	40	V	
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V	
Continuous Drain Current	$25^\circ\text{C}$	$I_D$	90	A
	$70^\circ\text{C}$		57	A
Pulsed Drain Current (NOTE 1)	$I_{D(pulse)}$	270	A	
Avalanche Current	$I_{AS}$	47	A	
Maximum Power Dissipation (NOTE 2)	$25^\circ\text{C}$	$P_D$	87	W
Single Pulse Avalanche Energy	EAS	110	mJ	
Operating Junction Temperature	$T_J$	150	$^\circ\text{C}$	
Storage Temperature	$T_{STG}$	-55-+150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

**ELECTRICAL CHARACTERISTICS** (TA = 25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX	Units
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>DS</sub> =250uA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 32V, V <sub>GS</sub> =0V T <sub>J</sub> =25°C			1	uA
		V <sub>DS</sub> = 32V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			5	uA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate threshold voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		2.5	V
Drain to Source On-state Resistance (note 2)	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A		5	6.5	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =20A		7	9	mΩ
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.8	1	V
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		1.4		Ω
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		341 5		pF
Output Capacitance	C <sub>OSS</sub>			282		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			210		pF
Total Gate Charge (10V)	Q <sub>G</sub>	V <sub>DD</sub> =32V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		30		nC
Gate-Source Charge	Q <sub>GS</sub>			7		nC
Gate-Drain Charge	Q <sub>GD</sub>			13		nC
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =20V, V <sub>GS</sub> =10V R <sub>G</sub> =3.3Ω, I <sub>D</sub> =20A		10		nS
Rise Time	T <sub>r</sub>			34		
Turn-Off Delay Time	T <sub>d(off)</sub>			56		
Fall Time	T <sub>f</sub>			15		
<b>DIODE CHARACERISTICS</b>						
Drain-Source Diode Forward Voltage (note 2)	V <sub>SD</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1.0	V
Continuous Source Current (note 1,3)	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current			90	A
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> =30A, T <sub>J</sub> =25°C di/dt=100A/us,		4.5		nS
Reverse Recovery Charge	Q <sub>rr</sub>			0.5		nC

Note 1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

Note 2. Pulse Test. Pulse width ≤ 300uS, Duty Cycle ≤ 1%.

Note 3. L=1mH, V<sub>DD</sub>=25V. I<sub>AS</sub>=47A. Starting T<sub>J</sub>=25°C



**TYPICAL CHARACTERISTICS**

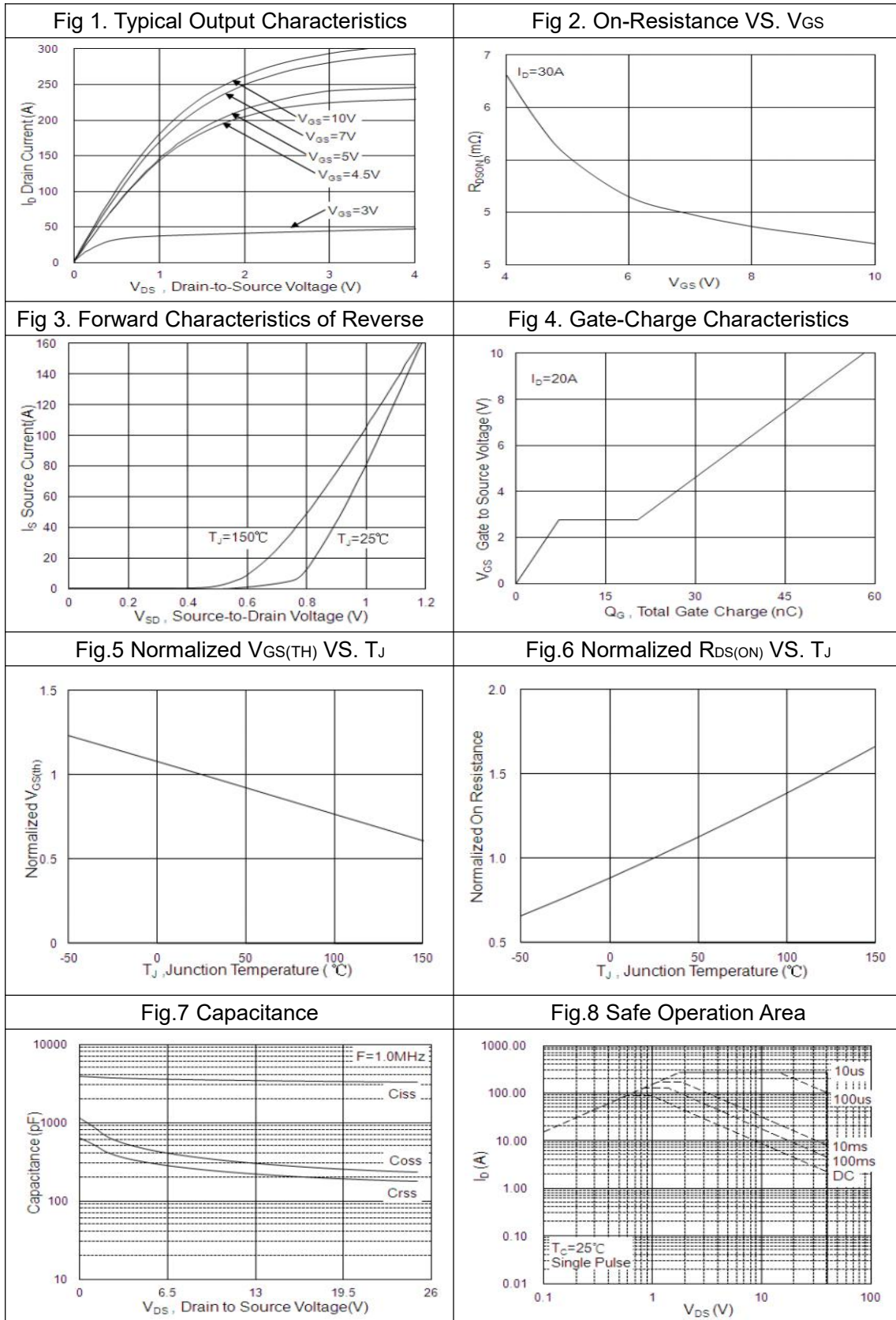
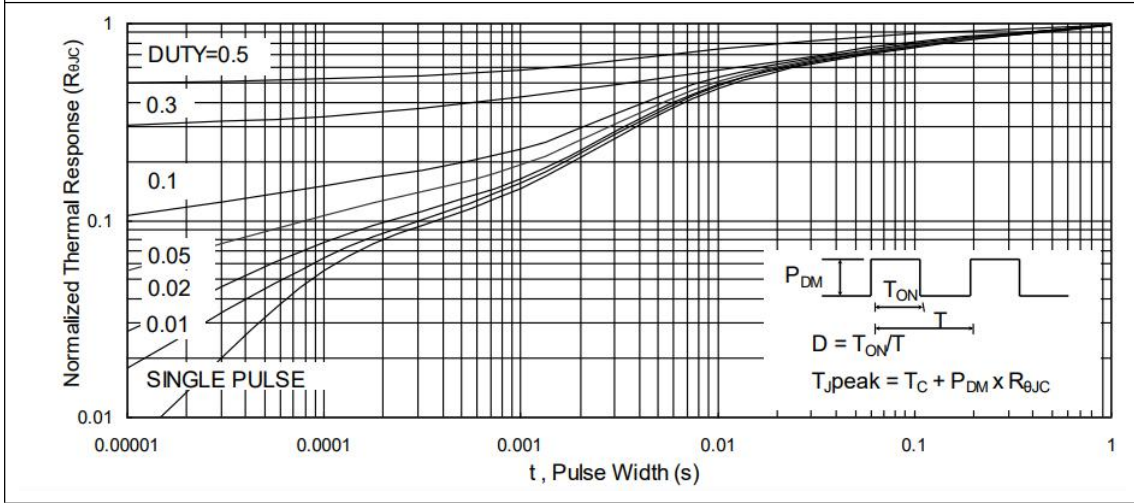
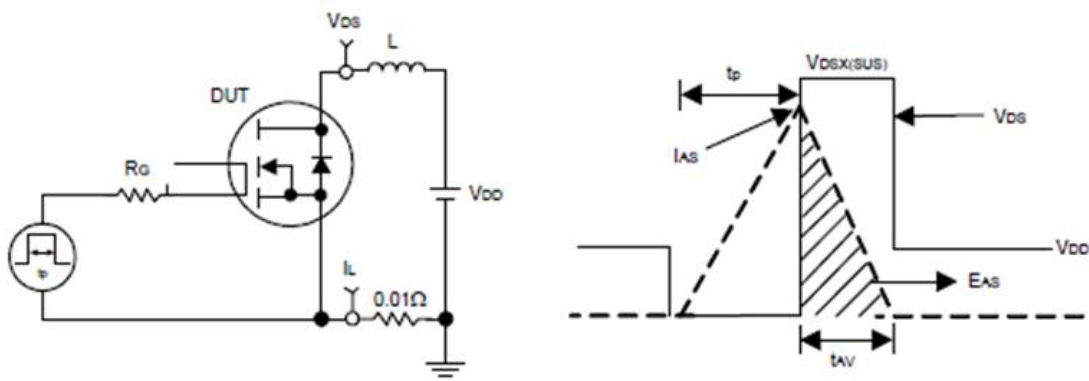




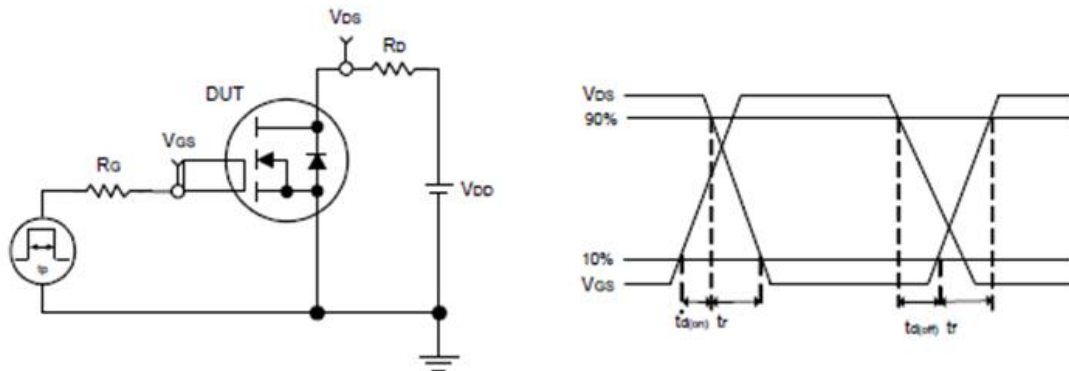
Fig.9 Normalized Maximum Transient Thermal Impedance



### Avalanche Test Circuit and Waveform



### Switching Time Test Circuit and Waveform





PACKAGE DIMENSIONS

TO-220

