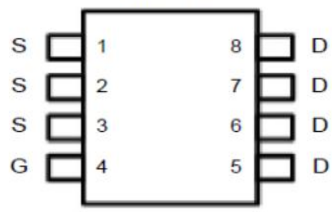
## GENERAL DESCRIPTION

The RZC3105 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

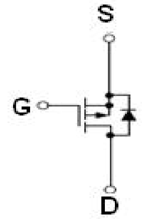
## PIN CONFIGURATION

Top View




SOP-8

Equivalent Circuit




P-Channel MOSFET

## FEATURES

- -30V/-8A, $R_{DS(ON)}$ =15mΩ $V_{GS}$ =-10V (MAX.)
- -30V/-8A, $R_{DS(ON)}$ =25mΩ $V_{GS}$ =-4.5V (MAX.)
- Super high density cell design for extremely low
- Exceptional on-resistance and maximum DC current capability
- Full RoHS compliance
- SOP-8 package design

## APPLICTIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

## ORDERING INFORMATION

| Part Number | Package | Top Marking | Packing |
|---|---|---|---|
| RZC3105 | SOP-8 | S3105 | 3000PCS/Real |

## MAXIMUM RATINGS (Ta = 25℃)

| Parameter | Symbol | | Value | Units |
|---|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | | -30 | V |
| Gate to Source Voltage | $V_{GSS}$ | | ±20 | V |
| Continuous Drain Current | 25℃ | $I_D$ | -8 | A |
| | 70℃ | | -6.4 | A |
| Pulsed Drain Current | $I_{D(pulse)}$ | | -32 | A |
| Maximum Power Dissipation | 25℃ | $P_D$ | 1.5 | W |
| Operating Junction Temperature | $T_J$ | | 150 | °C |
| Storage Temperature | $T_{STG}$ | | -55-+150 | °C |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | $T_L$ | | 260 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

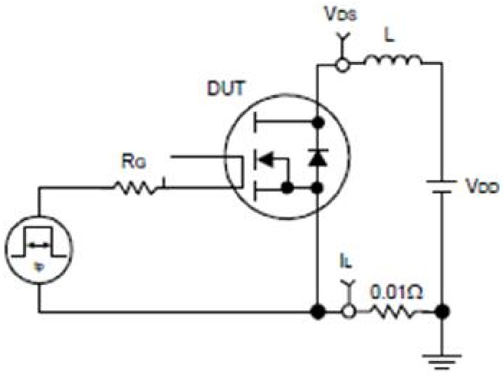
## ELECTRICAL CHARACTERISTICS (TA = 25℃)

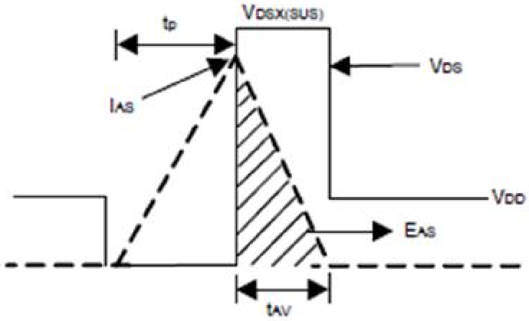
| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX | Units |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | BVDSS | $V_{GS}$=0V, $I_{DS}$=-250uA | -30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-30V,$V_{GS}$=0V | | | -1 | uA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | | | ±100 | nA |
| Gate threshold voltage | $V_{GS}$(th) | $V_{DS}$=$V_{GS}$,$I_D$=-250μA | | | -2.5 | V |
| Drain to Source On-state Resistance | $R_{DS(on)}$ | $V_{GS}$=-10V,$I_D$=-5.0A | | 12 | 15 | mΩ |
| | | $V_{GS}$=-4.5V,$I_D$=-5.0A | | 22 | 25 | mΩ |
| Drain-Source Diode Forward Voltage | $V_{SD}$ | $I_s$=1A,$V_{GS}$=0V | | 0.8 | 1.3 | V |
| Input Capacitance | Ciss | $V_{DS}$=-20V , $V_{GS}$=0V , f=1MHz | | 2220 | | pF |
| Output Capacitance | Coss | | | 305 | | pF |
| Reverse Transfer Capacitance | Crss | | | 235 | | pF |
| Total Gate Charge | Qg | $V_{DS}$=-20V , $V_{GS}$=-10V , $I_D$=-5A | | 22 | | nC |
| Gate-Source Charge | Qgs | | | 8.4 | | nC |
| Gate-Drain Charge | Qgd | | | 7.3 | | nC |

Note : 1. Pulse test: pulse width <= 300us, duty cycle<= 2%.

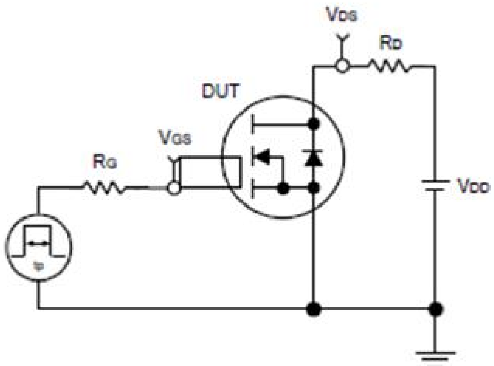
2. Static parameters are based on package level with recommended wire-bonding.

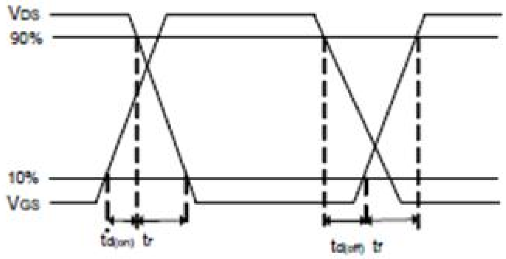
## Avalanche Test Circuit and Waveforms



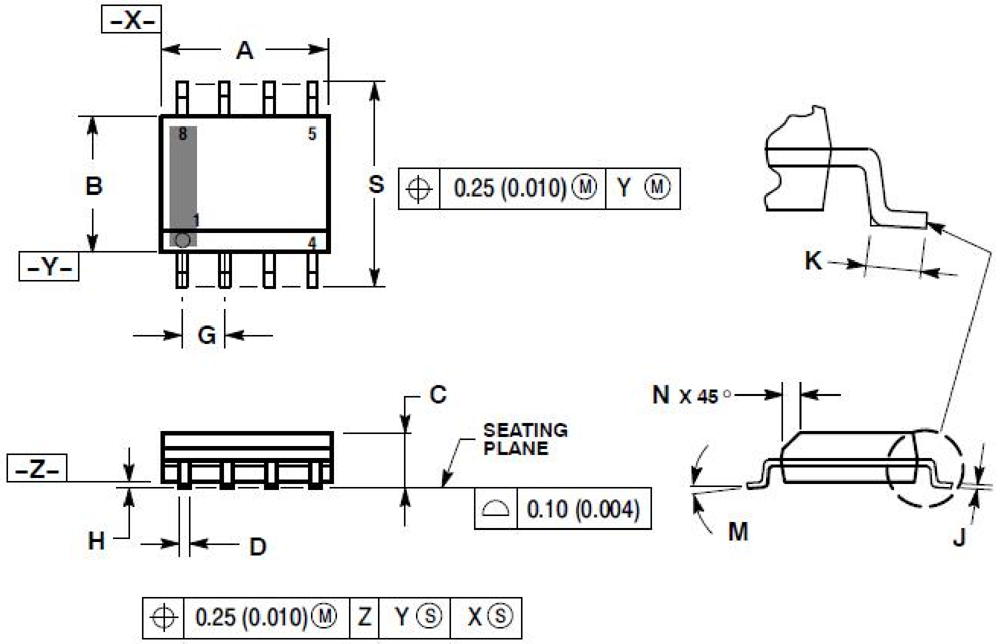

## Switching Time Test Circuit and Waveforms



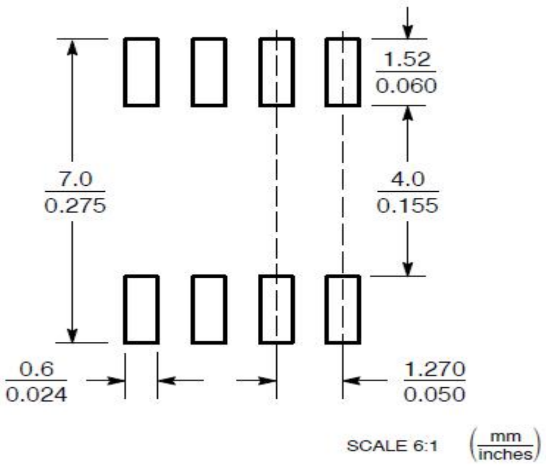



# PACKAGE DIMENSIONS

## SOP-8




SOLDERING FOOTPRINT*




| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |