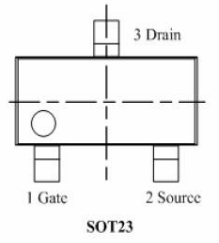
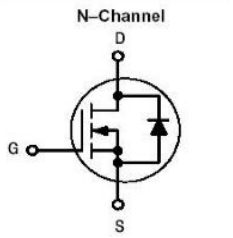
GENERAL DESCRIPTION

The RZC2317 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

PIN CONFIGURATION





FEATURES

- -20V/-4.7A, $R_{DS(ON)}$ =32mΩ V_{GS} =-4.5V (MAX.)
  $R_{DS(ON)}$ =40mΩ V_{GS} =-2.5V (MAX.)
  $R_{DS(ON)}$ =55mΩ V_{GS} =-1.8V (MAX.)
- Super high density cell design for extremely low
- Exceptional on-resistance and maximum DC current capability
- Full RoHS compliance
- SOT-23 package design

APPLICTIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

ORDERING INFORMATION

Part Number	Package	Top Marking	Packing
RZC2317	SOT-23	2317	3000PCS/Real

MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol		Value	Units
Drain to Source Voltage	V_{DSS}		-20	V
Gate to Source Voltage	V_{GSS}		±12	V
Continuous Drain Current	25℃	I_D	-4.7	A
	70℃		-3.8	A
Pulsed Drain Current	$I_{D(pulse)}$		-18.8	A
Maximum Power Dissipation	25℃	P_D	1	W
Thermal Resistance,Junction to Case	$R_{\theta JC}$		125	℃/W
Thermal Resistance,Junction to Ambient	$R_{\theta JA}$		80	℃/W
Operating Junction Temperature	T_J		150	°C
Storage Temperature	T_{STG}		-55-+150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)	T_L		260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

ELECTRICAL CHARACTERISTICS (TA = 25℃)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{DS}=-250uA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V,V_{GS}=0V			-1	uA
Gate Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V			±100	nA
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=-250μA			-2.5	V
Drain to Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V,I_D=-4.0A		25	32	mΩ
		V_{GS}=-2.5V,I_D=-2.0A		32	40	
		V_{GS}=-1.8V,I_D=-1.5A		42	55	
Input Capacitance	Ciss	V_{DS}=-15V , V_{GS}=0V , f=1MHz		2280	3192	pF
Output Capacitance	Coss			220	308	pF
Reverse Transfer Capacitance	Crss			187	262	pF
Total Gate Charge	Qg	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-4A		27	38	nC
Gate-Source Charge	Qgs			3.6	5.0	nC
Gate-Drain Charge	Qgd			6.5	9	nC
Turn-On Delay Time	Td(on)	V_{DS}=-15V, V_{GS}=-10V R_G=3.3Ω,I_D=-1A		9.2	18.4	nS
Rise Time	Tr			59	106	
Turn-Off Delay Time	Td(off)			99	198	
Fall Time	Tf			71	142	
Drain-Source Diode Forward Voltage	V_{SD}	Is=-1A,V_{GS}=0V, TC=25℃			-1.0	V
Maximum Continuous Drain-Source Diode Forward Current	I_D	T_C=25℃			-4.7	A
Maximum Pulse Drain-Source Diode Forward Current	I_{DSM}				-18.8	A
Reverse Recovery Time	trr	IF=-4A,T_J=25℃ Di/Dt=100A/uS		52		nS
Reverse Recovery Charge	Qrr			28		nC

Note : 1.The data tested by surface mounted on a 1 $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≦300us , duty cycle ≦ 2%

3.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

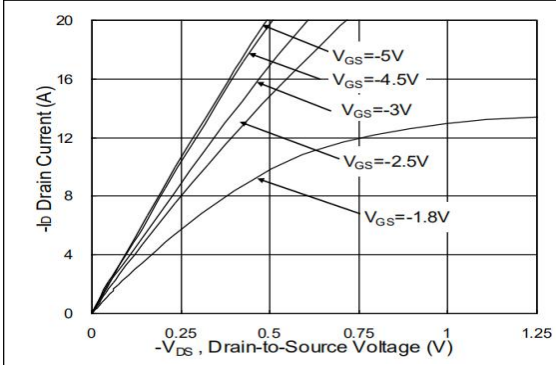


Fig 2. On-Resistance VS. VGS

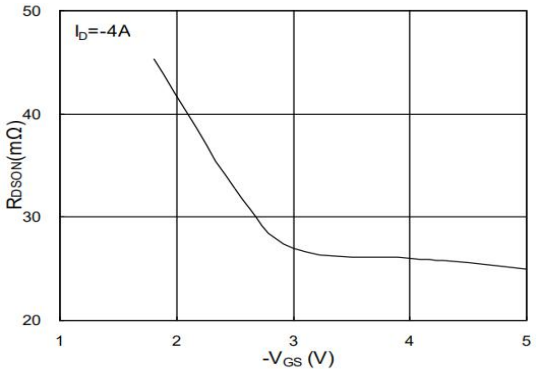


Fig 3. Forward Characteristics of Reverse

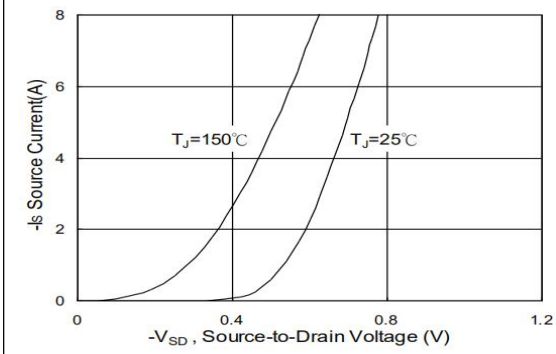


Fig 4. Gate-Charge Characteristics

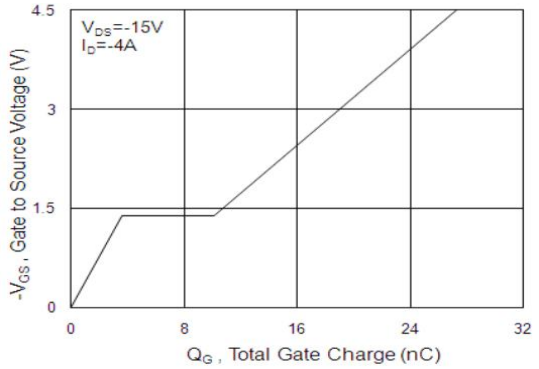


Fig.5 Normalized VGS(TH) VS. TJ

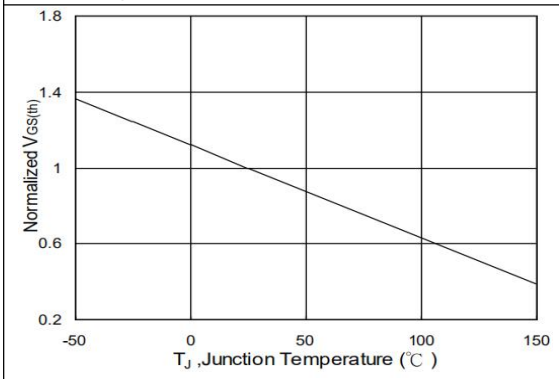


Fig.6 Normalized RDS(ON) VS. TJ

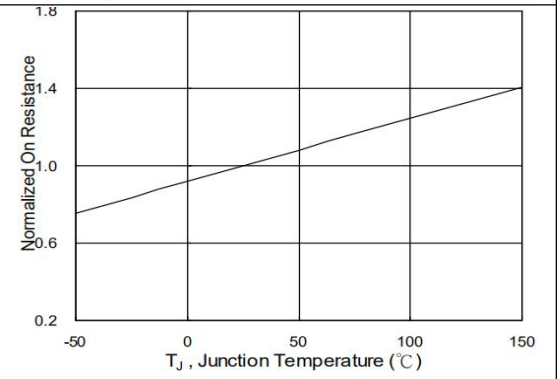


Fig.7 Capacitance

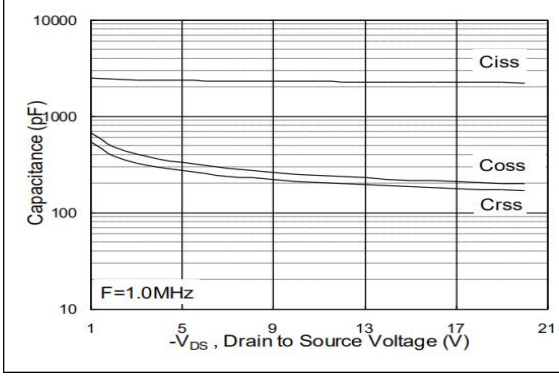


Fig.8 Safe Operation Area

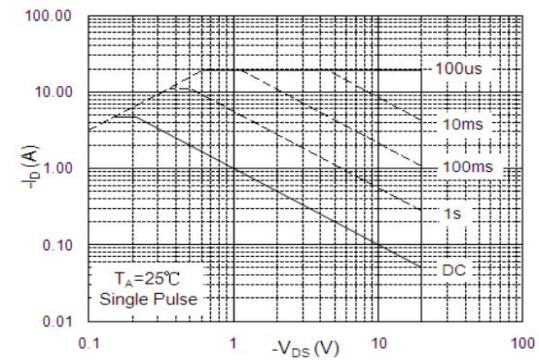
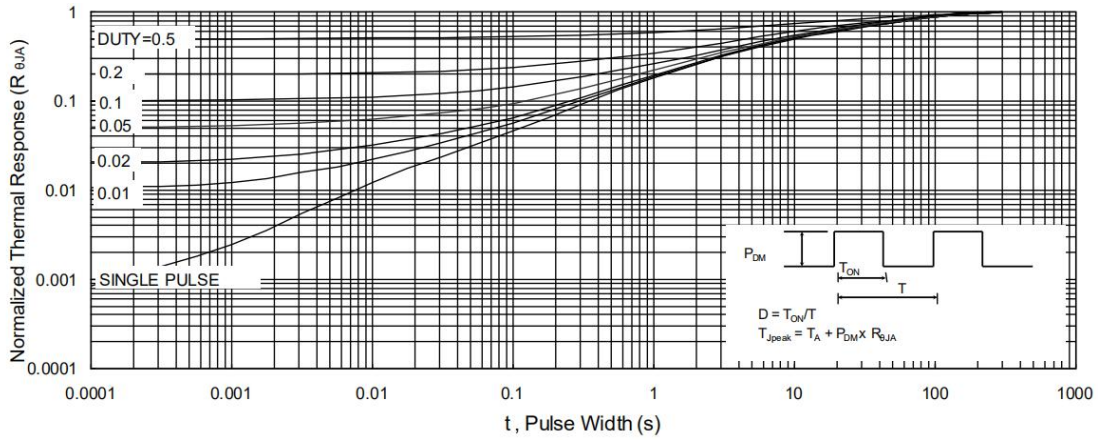
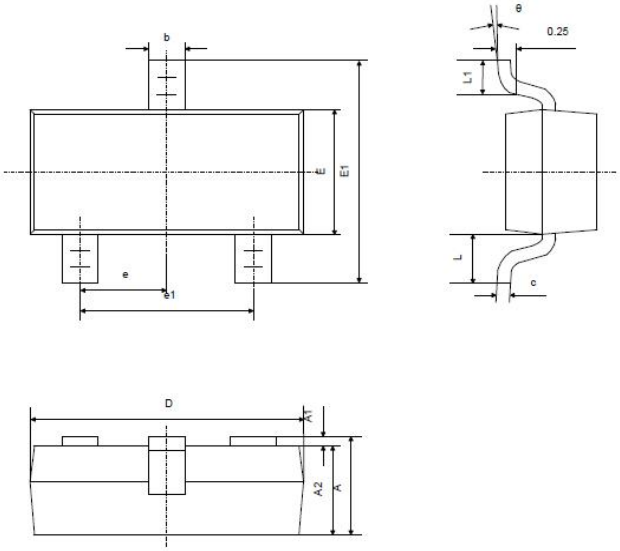


Fig.9 Maximum Effective Transient Thermal Impedance,Junction to Case



PACKAGE DIMENSIONS

SOT-23



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

Note:

1. Dimension D does not include mold flash, protrusions or gate burrs. mold flash, protrusions or gate burrs shall not exceed 0.10mm per side.
2. Dimension E1 does not include inter-lead flash or protrusion. Inter-lead flash or protrusion shall not exceed 0.1mm per side.