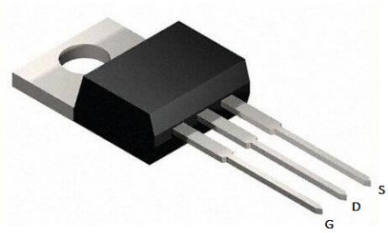
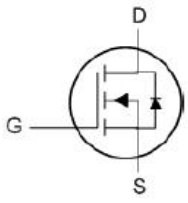
GENERAL DESCRIPTION

The RZC0014T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

PIN CONFIGURATION





FEATURES

- 100V/75A, $R_{DS(ON)}$ =14mΩ @V_{GS} = 10V (TPY.)
- Super high density cell design
- 100% EAS guaranteed
- Super low gate charge
- Exceptional on-resistance and maximum DC current capability
- Full RoHS compliance
- TO-220 package design

APPLICTIONS

- Power Adapter in Note book
- Synchronous Rectification
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

ORDERING INFORMATION

Part Number	Package	Top Marking
RZC0014T	TO-220	T0014
RZC0014TF	TO-220F	TF0014

MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol		Value	Units
Drain to Source Voltage	V_{DSS}		100	V
Gate to Source Voltage	V_{GSS}		±20	V
Continuous Drain Current,V_{GS}@10V[1,6]	25℃	I_D	75	A
	100℃		60	A
Pulsed Drain Current[2]	$I_{D(pulse)}$		300	A
Single Pulse Avalanche Energy[3]	EAS		125	mJ
Maximum Power Dissipation[4]	25℃	P_D	87	W
Operating Junction Temperature	T_J		-55-+150	°C
Storage Temperature	T_{STG}		-55-+150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)	T_L		260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

THERMAL DATA

Parameter	Symbol	Typ.	Value	Units
Thermal Resistance Junction-Ambient[1]	$R_{\theta JA}$	---	62	°C/W
Thermal Resistance Junction-Case[1]	$R_{\theta JC}$	---	0.84	°C/W

ELECTRICAL CHARACTERISTICS (TA = 25℃,unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{DS}=250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= 100V, V_{GS}=0V,T_J=25℃			1	uA
		V_{DS}= 100V, V_{GS}=0V,T_J=85℃			30	uA
Gate Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D= 250μA		2	2.5	V
Drain to Source On-state Resistance[2]	$R_{DS(ON)}$	V_{GS}=10V,I_D=8A		14	16	mΩ
Input Capacitance	C_{ISS}	V_{DS}=20V , V_{GS}=0V , f=1MHz		4708		pF
Output Capacitance	C_{OSS}			326		pF
Reverse Transfer Capacitance	C_{RSS}			247		pF
Total Gate Charge (10V)	Qg	V_{DS}=32V , V_{GS}=10V , I_D=20A		75		nC
Gate-Source Charge	Qgs			15.5		nC
Gate-Drain Charge	Qgd			20.3		nC

DIODE CHARACERISTICS

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain-Source Diode Forward Voltage	V_{SD}	Is=1A,V_{GS}=0V			1.2	V
Continuous Source Current[1,5]	Is	V_G=V_D=0V, Force Current			75	A
Reverse Recovery Time	trr	I_F=30A,TJ=25℃ di/dt=100A/us,		28		nS
Reverse Recovery Charge	Qrr			50		nC

Note :

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

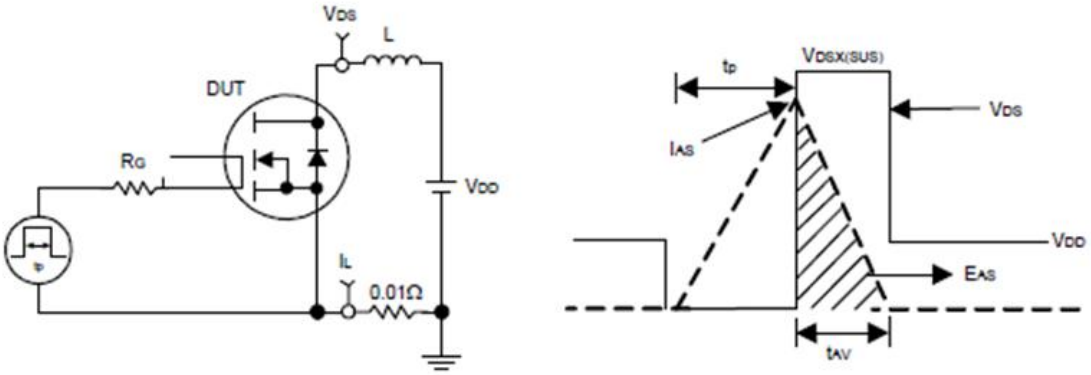
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=50A

4.The power dissipation is limited by 150℃ junction temperature

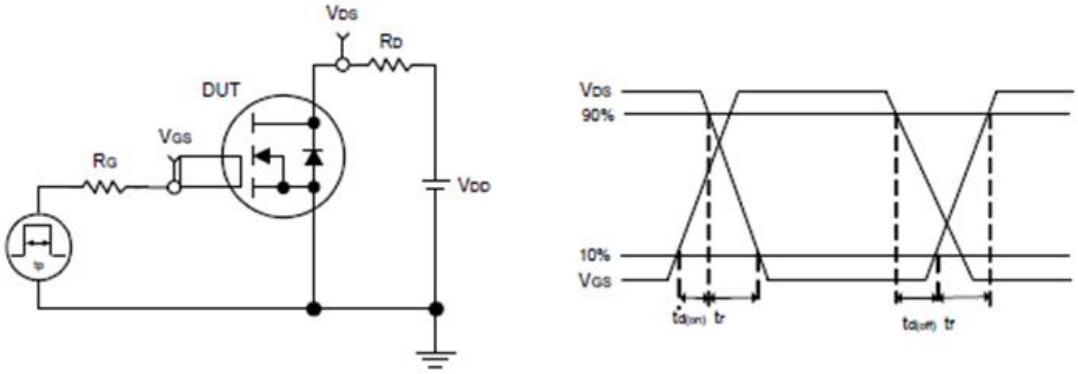
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

6.Package limitation current is 85A.

Avalanche Test Circuit and Waveforms

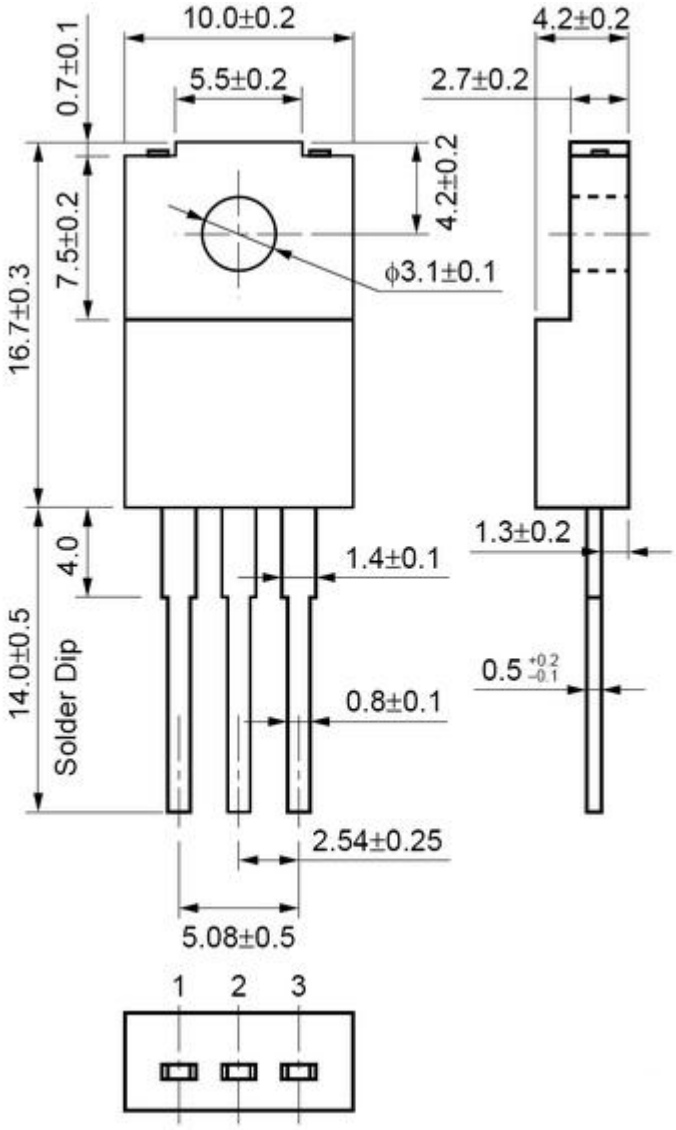


Switching Time Test Circuit and Waveforms

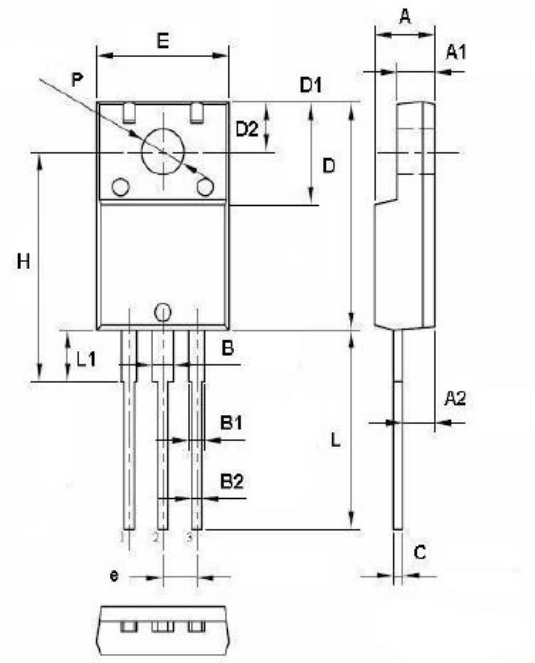


PACKAGE DIMENSIONS

TO-220



TO-220F



TO-220F DIMENSION				
Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.200	4.800	0.165	0.189
A1	2.500	3.100	0.098	0.122
A2	2.100	2.700	0.083	0.106
B	1.300	1.900	0.051	0.075
B1	0.900	1.500	0.035	0.059
B2	0.650	1.050	0.026	0.041
C	0.400	1.000	0.016	0.039
D	15.700	16.300	0.618	0.642
D1	6.900	7.500	0.272	0.295
D2	3.200	3.800	0.126	0.150
E	9.700	10.300	0.382	0.406
e	2.350	2.750	0.093	0.108
H	15.800	16.400	0.622	0.646
L	13.500	14.500	0.531	0.571
L1	3.400	3.800	0.134	0.150