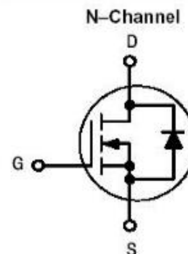
GENERAL DESCRIPTION

The RZC0014D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

PIN CONFIGURATION



FEATURES

- 100V/60A, $R_{DS(ON)}$ =14mΩ @V_{GS} = 10V (TPY.)
- Super high density cell design
- 100% EAS guaranteed
- Super low gate charge
- Exceptional on-resistance and maximum DC current capability
- Full RoHS compliance
- TO-252 package design

APPLICTIONS

- Power Adapter in Note book
- Synchronous Rectification
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

ORDERING INFORMATION

Part Number	Package	Top Marking	Packing
RZC0014D	TO-252	D0014	2500PCS/Tape&Real

MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol		Value	Units
Drain to Source Voltage	V_{DSS}		100	V
Gate to Source Voltage	V_{GSS}		±20	V
Continuous Drain Current, V_{GS}@10V[1,6]	25℃	I_D	60	A
	100℃		48	A
Pulsed Drain Current[2]	$I_{D(pulse)}$		200	A
Single Pulse Avalanche Energy[3]	EAS		125	mJ
Maximum Power Dissipation[4]	25℃	P_D	52	W
Operating Junction Temperature	T_J		-55-+150	°C
Storage Temperature	T_{STG}		-55-+150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)	T_L		260	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

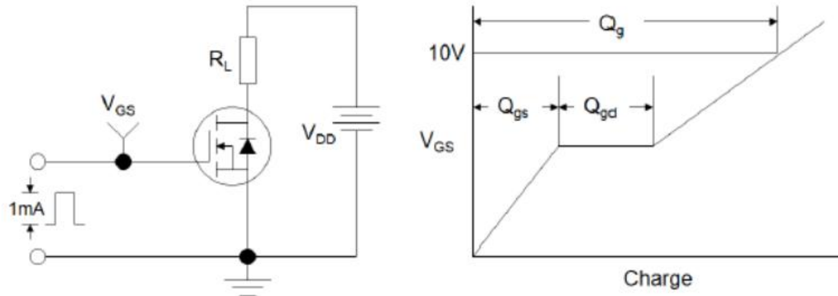
ELECTRICAL CHARACTERISTICS (TA = 25℃,unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{DS}=250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V,T_J=25℃			1	uA
		V_{DS}= 100V, V_{GS}=0V,T_J=85℃			30	uA
Gate Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D= 250μA		2	2.5	V
Drain to Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=8A		14	16	mΩ
Input Capacitance	C_{ISS}	V_{DS}=20V , V_{GS}=0V , f=1MHz		4708		pF
Output Capacitance	C_{OSS}			326		pF
Reverse Transfer Capacitance	C_{RSS}			247		pF
Total Gate Charge	Qg	V_{DS}=32V , V_{GS}=10V , I_D=20A		75		nC
Gate-Source Charge	Qgs			15.5		nC
Gate-Drain Charge	Qgd			20.3		nC

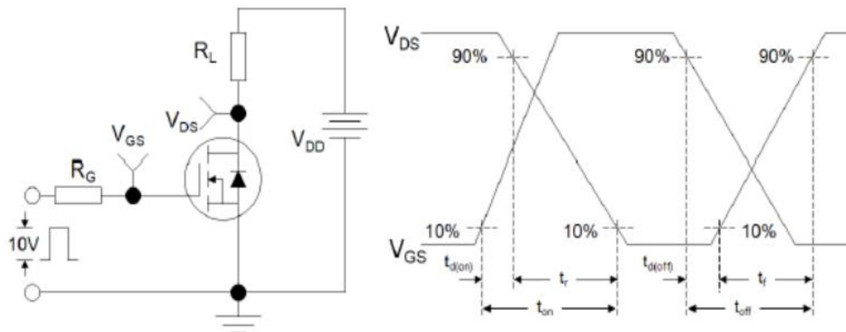
Diode Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX	Units
Drain-Source Diode Forward Voltage	V_{SD}	Is=1A,VGS=0V			1.2	V
Continuous Source Current	Is	VG=VD=0V,Force Current			60	A
Reverse Recovery Time	trr	IF=20A,dI/dt=100A/us ,TJ=25℃		28		nS
Reverse Recovery Charge	Qrr			50		nC

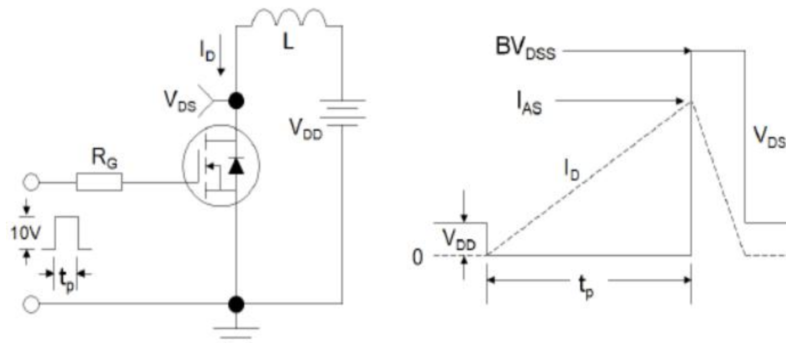
Gate Charge Test Circuit and Waveform



Resistive Switching Test Circuit and Waveform

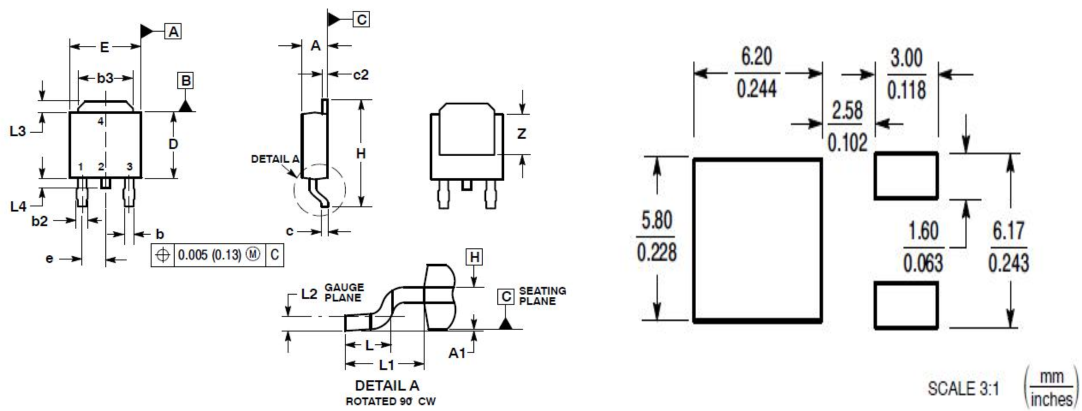


Unclamped Inductive Switching Test Circuit and Waveform



PACKAGE DIMENSIONS

TO-252



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---